ISEDA 2027 International Symposium of EDA

May 21-24, 2027 | Shangri-La Beijing, Beijing, China

Call For Papers

Scope

The International Symposium of EDA (ISEDA) is an annual forum dedicated to VLSI design automation. ISEDA 2027 will be held in Beijing, China, on May 21-24, 2027. We invite original contributions that address challenges in electronic design automation, present advances in design technologies, and explore future research directions. The symposium covers the full range of EDA topics, from device and circuit levels to the system level, including analog and digital design, manufacturing, and emerging applications. We welcome academic and industrial researchers and developers working on both the theory and practice of EDA.

▶ ***Advisors***
IEEE-CEDA ACM-SIGDA

▶ ***Organizer***
EDA Ecosystem Development Accelerator (EDA²)

▶ ***Co-organizer***
Peking University

Submission

▶ Invited talks: An abstract of up to one page
Extended abstracts: 1-2 pages
Regular papers: 4-6 pages

▶ Please make sure there is NO AUTHOR INFORMATION in your submission, and you can download the paper template through the website: https://www.eda2.com/iseda/sub.html

▶ Best Paper Award, Honorable Mention Paper Award will be selected after the presentations.

▶ Submit your paper through the link or QR Code:
https://www.eda2.com/conferenceHome/submissionHome

▶ ***Important Dates***

- Deadline for regular paper submission
  February 24, 2027
- Notification of acceptance
  March 31, 2027
- Deadline for final version
  April 24, 2027
- Deadline for invited talks, extended abstracts, tutorials, special sessions and industry sessions
  March 31, 2027

Areas of Interest *(Original papers in, but not limited to, the following areas are invited.)*

[1] System-Level Modeling and Design Methodology
1.1 HW/SW co-design, co-simulation and co-verification
1.2 System-level design exploration, synthesis and optimization
1.3 System-level formal verification
1.4 System-level modeling, simulation and validation
1.5 Networks-on-chip and NoC-based system design
1.6 Hardware construction using Scala-embedded languages

[2] Memory Architecture and Near/In-Memory Computing
2.1 Storage systems and memory architecture
2.2 On-chip memory architectures and management: scratch-pads, compiler-controlled memories, etc.
2.3 Memory/storage hierarchies and management for emerging memory technologies
2.4 Near-memory and in-memory computing

[3] Analog and Mixed-Signal Design Automation
3.1 Analog/mixed-signal/RF synthesis
3.2 Analog layout, verification and simulation techniques
3.3 High-frequency electromagnetic simulation of circuits
3.4 Mixed-signal design considerations

[4] High-Level, Behavioral, and Logic Synthesis and Optimization
4.1 Digital simulation and emulation
4.2 High-level synthesis
4.3 Logic synthesis
4.4 Synthesis for approximate computing

[5] Analysis and Optimization for Power and Timing
5.1 Deterministic/statistical timing analysis and optimization
5.2 Process technology modeling for timing analysis
5.3 Power modeling, analysis and simulation
5.4 Low-power design and optimization at circuit and system levels
5.5 Thermal-aware design and dynamic thermal management
5.6 Energy harvesting and battery management

[6] Physical Implementation
6.1 Floorplanning, partitioning, placement and routing optimization
6.2 Interconnect planning and synthesis
6.3 Clock network synthesis
6.4 Physical design of 3D/2.5D ICs and packages (e.g., TSV, interposer, monolithic)
6.5 Post-layout and post-silicon optimization
6.6 Layout verification

[7] Testing, Validation, Simulation, and Verification
7.1 RTL and gate-level modeling, simulation and verification
7.2 Circuit-level formal verification
7.3 ATPG, BIST and DFT
7.4 System test and 3D IC test, online test and fault tolerance
7.5 Memory test and repair

[8] Design for Manufacturability and Reliability
8.1 Design-technology co-optimization (DTCO)
8.2 Standard and custom cell design and optimization
8.3 Reticle enhancement, lithography-related design optimization and design rule checking
8.4 Design for manufacturability, yield, defect tolerance, cost issues and DFM impact
8.5 Device-, gate- and circuit-level reliability analysis and optimization (e.g., soft errors, aging)
8.6 Post-layout optimization

[9] Packaging and Multi-Physics Simulation
9.1 Extraction, TSV and package modeling
9.2 Chiplet design and design tools
9.3 Chip-level thermal simulation
9.4 Packaging stress analysis
9.5 Multi-physics simulation
9.6 Signal/power integrity, EM modeling and analysis

[10] Technology and Modeling
10.1 Device compact modeling
10.2 Process design kits
10.3 Semiconductor process and device simulation
10.4 Cell library design, characterization and verification
10.5 New transistor/device and process technologies: spintronic, phase-change, single-electron, 2D materials, etc.

[11] Emerging Technologies and Applications
11.1 Biomedical, biochip, nanotechnology and MEMS
11.2 Design automation for 3D ICs and heterogeneous integration
11.3 Design automation for quantum computing
11.4 Design automation for silicon photonics
11.5 Design automation and verification for compound semiconductors

[12] AI and Open Source EDA
12.1 Artificial intelligence for EDA
12.2 Cloud and parallel computing for EDA
12.3 Open source EDA
12.4 EDA databases
12.5 EDA standardization

Committee

▶ ***Executive Committee***

General Chairs
- Yue Hao, Xidian University, Academician of the Chinese Academy of Sciences
- Runsheng Wang, Peking University

▶ ***Organizing Committee***

Conference Chairs
- Yun Liang, Peking University
- Ulf Schlichtmann, Technical University of Munich
- Tsung-Yi Ho, The Chinese University of Hong Kong

Technical Program Chairs
- Yibo Lin, Peking University
- Georges Gielen, KU Leuven

Contact Us

▶ Paper submission: Joyce Zhong (iseda@eda2.com)
▶ EDA²: Qiuping Huang (conference_affairs@eda2.com)
▶ Venue: Shangri-La Beijing, Beijing, China

▶ Conference website
https://www.eda2.com/iseda/index.html