ISEDA 2025

International Symposium of EDA

May 9-12, 2025 Hong Kong Disneyland, China

Conference Program

TABLE OF CONTENTS

WELCOME MESSAGE

Welcome to the 2025 International Symposium of EDA!

It is my immense pleasure to welcome you to this year's ISEDA, taking place for the first time in Hong Kong. This historic decision reflects, in part, the ISEDA Executive Committee's recognition of Hong Kong's strong commitment to advancing semiconductor technologies, where the ISEDA community will play a pivotal role. We are thrilled to have you join us for this exciting event, uniting thought leaders, innovators, and passionate individuals from around the globe.

Sponsored by IEEE and ACM, and jointly organized by EDA^2 and the EDA Committee of CIE, the ISEDA remains the premier venue for researchers and practitioners to share ground-breaking ideas and technological innovations in advancing cutting-edge computer-aided design techniques for microelectronics, devices, circuits, architectures, systems, and applications in this dynamic era of artificial intelligence. Here, you will encounter leading-edge R&D solutions and identify future research directions. We encourage you to engage in dynamic discussions with other attendees and explore new collaborative opportunities.

This year has set a new record for paper submissions, with 214 entries across 12 technical tracks from 7 regions and countries. To ensure a thorough review process, we invited 181 exceptional experts as our Technical Program Committee members. Accepted papers are organized into 27 technical sessions, alongside 2 special sessions and 7 embedded tutorials that provide in-depth insights from established experts. We are also hosting three panels on a range of compelling topics, such as 'AI/LLM for IC Manufacturing', 'Scaling up AI-Assisted EDA Techniques with Large Foundation AI Models', and 'The Fusion of AI and Multiphysics: Accelerating EDA Revolution'. These panels will provide an excellent opportunity for more in-depth interaction. We encourage you to participate and consider extending your stay to engage with these panels.

Keynotes are a highlight of ISEDA, and we are honoured to feature ten distinguished speakers this year. Saturday's keynote will be delivered by Dr. Giovanni De Micheli from École polytechnique fédérale de Lausanne, Dr. Georges Gielen from Katholieke Universiteit Leuven, and Dr. Hong Zhou from Huawei. On Sunday, Dr. Sung Kyu Lim from Georgia Institute of Technology, Dr. Ulf Schlichtmann from Technical University of Munich and Dr. Jinjun Xiong from University at Buffalo will deliver keynote talks. Monday's keynote will be delivered by Dr. Tim Cheng from The Hong Kong University of Science and Technology, Dr. Sachin S. Sapatnekar from the University of Minnesota, Dr. Jaijeet Roychowdhury from University of California, Berkeley and Dr. Vijay Janapa Reddi from Harvard University.

The success of ISEDA hinges on your participation. We hope you will reconnect with old friends and forge new connections. Additionally, we invite you to enjoy an exciting social event in Hong Kong Disneyland Hotel, a venue that seamlessly combines sophistication, modern amenities, and the enchanting charm of Disney. Please make the most of your time here by exploring all the incredible activities Hong Kong has to offer.

Lastly, I want to extend heartfelt gratitude to our generous sponsors, dedicated supporters, and tireless volunteers that include members of the executive committee, technical program committee, and numerous student activity organizers. Your collective efforts have made this year's ISEDA a reality. Thank you!

Looking forward to an inspiring event!

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Dr. Runsheng Wang
Peking University

Dr. Gang Qu
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[12] AI & Open Source EDA

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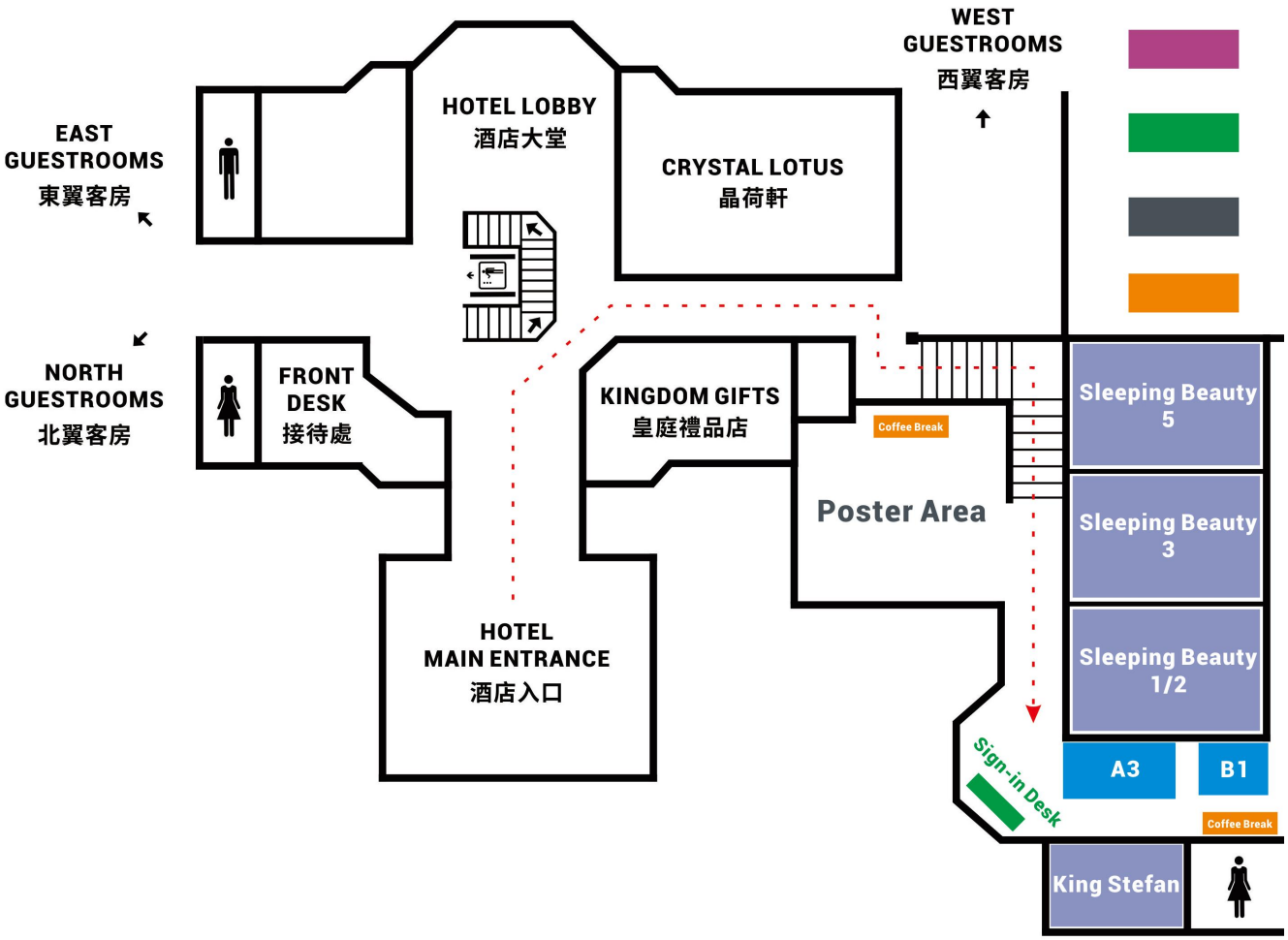
CONFERENCE VENUE

Hong Kong Disneyland Hotel

Address: Hong Kong Disneyland Resort, Lantau Island, Hong Kong



Hong Kong Disneyland Hotel

Conference Board

Partner Exhibitor

Sign-in Desk

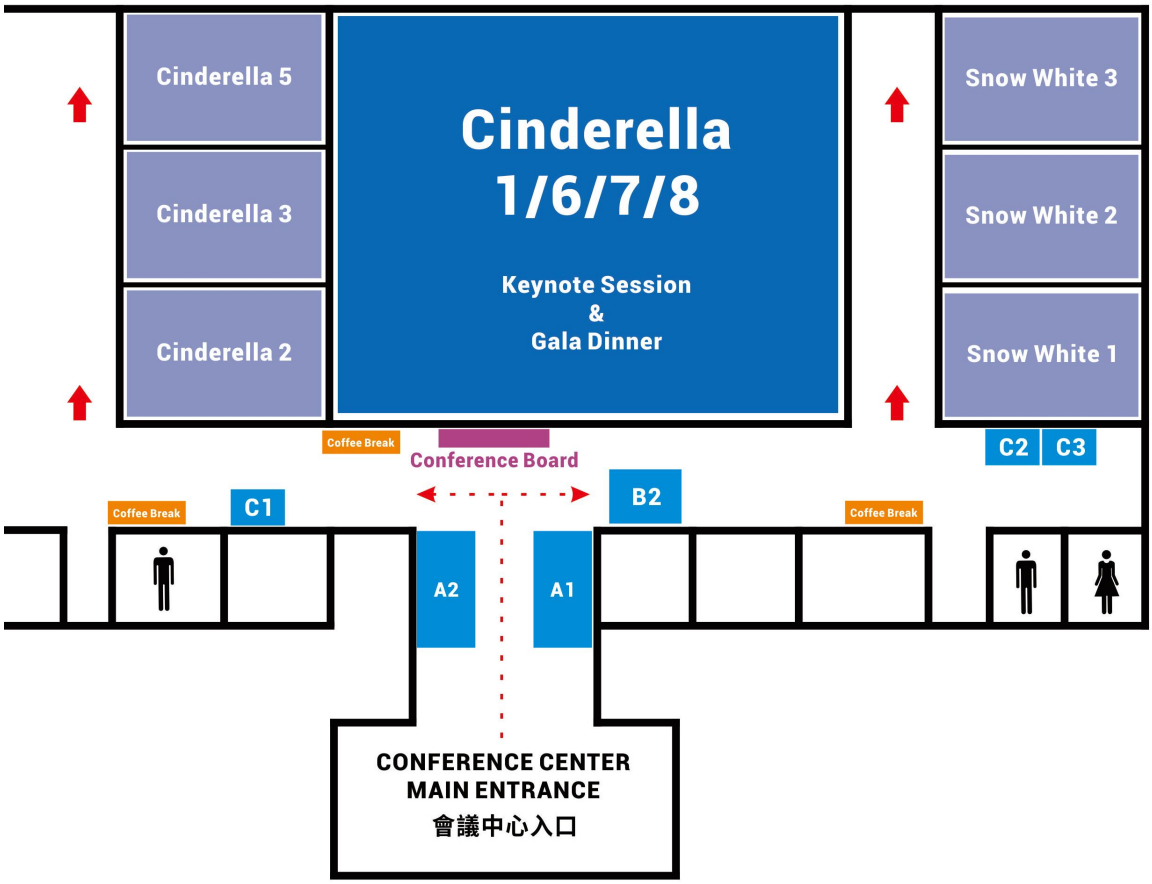
A1	Semitronix	A2	Empyrean	A3	EDA²

Poster Area

B1	PRIMARIUS	B2	UNIVISTA

Coffee Break

C1	Easylogic	C2	XPEEDIC	C3	S2C



AGENDA OVERVIEW

Sign-in & Conference Materials Collection	**May 09 | 11:00-20:00** **May 10 | 08:00-18:00** **May 11 | 08:00-16:00** **May 12 | 08:00-13:00** Conference Center @ Disneyland Hotel

May 9, 2025 | Friday		
12:00-14:00	Lunch @ Enchanted Garden Restaurant	
14:00-17:00	**Tutorial 1** Test and Health Monitoring under Approximations and Variations	Snow White 1
	Tutorial 2 Advanced Open-Source FPGA HLS and Physical Implementation Tools	Cinderella 3
	Tutorial 3 VLSI Physical Design, From 2D to 3D	Cinderella 2
	Tutorial 4 AHS: An EDA toolbox for Agile Chip Front-end Design	Sleeping Beauty 3
	Tutorial 5 Formal Verification for EDA	Sleeping Beauty 5
	Tutorial 6 LLM Applications in EDA	Sleeping Beauty 1/2
	Tutorial 7 AI-Driven Breakthroughs in Next-Generation Circuit Simulation and Reliability	Snow White 2/3
15:20-15:40	Break	Foyer

May 10, 2025 | Saturday		
08:00-08:30	Morning Coffee & Tea	Foyer
08:30-09:00	**Opening Ceremony & Announcement of ISEDA 2026**	Cinderella Ballroom
	Keynote Speech 1 & 2 Host: **Xin Li**, Duke Kunshan University	
09:00-09:40	**Prof. Giovanni De Micheli**, École polytechnique fédérale de Lausanne (EPFL) **Speech Title**: The Future of Computing Systems Design	
09:40-10:20	**Prof. Georges Gielen**, Katholieke Universiteit Leuven (KU Leuven) **Speech Title**: DeepDesignAMS: Will Tomorrow's Analog Integrated Circuits be Generated by AI?	
10:20-10:40	Break	Foyer
10:40-12:00	**Technical Session 1** System-Level Simulation, Modeling, and Co-Verification	Sleeping Beauty 1/2
	Technical Session 2 Innovative Simulation and Data Compression for Verification	Snow White 2/3
	Technical Session 3 Emerging Transistor Technologies and Novel Process Innovations	Sleeping Beauty 5
	Technical Session 4 Emerging Technologies and Applications in EDA	Snow White 1
	Technical Session 5 Large Language Models and Next-Generation EDA Tools	Sleeping Beauty 3
12:00-14:00	Lunch & Keynote Speech	Cinderella Ballroom
12:30-12:40	**Address** from Special Guest **Mr. Albert Wong**, Hong Kong Science and Technology Parks Corporation	
	Keynote Speech 3 Host: **Yu Huang**, HiSilicon Technologies Co., Ltd.	
12:40-13:20	**Dr. Hong Zhou**, Institute of Strategic Research, Huawei **Speech Title**: Building a Better Connected and Intelligent World with STCO Collaborative Development	
14:00-15:40	**Technical Session 6** Analog/Mixed-Signal Synthesis and Layout Optimization	Snow White 1
	Technical Session 7 High-Level and Behavioral Synthesis: Trends and Optimization	King Stefan
	Technical Session 8 Physical Design and 3D/2.5D Integration Techniques	Sleeping Beauty 3
	Technical Session 9 Reliability Engineering and Post-Layout Optimization	Snow White 2
	Technical Session 10 AI-Driven Design Automation and Open Source Initiatives	Sleeping Beauty 1/2

14:00-15:40	**Special Session 1** CEDA-adjoint Special Session: Deep Learning Inspired Algorithms for Physical Modeling and Analysis of Advanced IC Design	Snow White 3
	Panel 1 Scaling up AI-Assisted EDA Techniques with Large Foundation AI Models	Sleeping Beauty 5
15:40-16:00	Break	Foyer
15:40-16:00	**Poster Session** @ Poster Area of Conference Center @ Disneyland Hotel	
16:00-18:00	**Technical Session 11** Innovations in Memory Architecture and Near/In-Memory Computing	Snow White 3
	Technical Session 12 Advanced Floorplanning and Macro Placement	Sleeping Beauty 1/2
	Technical Session 13 Design-Technology Co-Optimization and Manufacturability	King Stefan
	Technical Session 14 Efficient Parameter Extraction and Modeling Techniques	Snow White 1
	Technical Session 15 Large Language Models and Next-Generation EDA Tools	Snow White 2
	Special Session 2 Bridging AI and Hardware: Advancing Specialized Circuits, Design Automation, and Manufacturing	Sleeping Beauty 3
	Panel 2 AI/LLM for IC Manufacturing	Sleeping Beauty 5
18:30-21:00	**Gala Dinner Sponsored by AMEDAC**	Cinderella Ballroom

May 11, 2025 | Sunday		
08:30-09:00	Morning Coffee & Tea	Foyer
	Keynote Speech 4 & 5 Host: **Tsung-Yi Ho**, The Chinese University of Hong Kong	Cinderella Ballroom
09:00-09:40	**Prof. Sung Kyu Lim**, Georgia Institute of Technology (Gatech) **Speech Title**: Enhancing AI Chip Design: AI and Traditional Algorithms for Multi-Chip Integration	
09:40-10:20	**Prof. Ulf Schlichtmann**, Technical University of Munich (TUM) **Speech Title**: Optical Networks-on-Chip: EDA for the Future of Interconnect	
10:20-10:40	Break	Foyer
10:40-12:00	**Technical Session 16** Power Modeling, Analysis, and Thermal Management	Sleeping Beauty 1/2
	Technical Session 17 Advanced Test Methodologies and DFT Techniques	Sleeping Beauty 3
	Technical Session 18 Device Compact Modeling and Process Simulation	Sleeping Beauty 5
	Technical Session 19 Emerging Technologies and Applications in EDA	Snow White 2/3
12:00-14:00	Lunch & Keynote Speech	Cinderella Ballroom
	Keynote Speech 6 Host: **Tsung-Yi Ho**, The Chinese University of Hong Kong	
12:30-13:10	**Prof. Jinjun Xiong**, University at Buffalo **Speech Title**: A Reflection on Machine Learning for EDA: What are Possible Future Directions?	
13:10-13:30	**Invited Talk** from **Ms. Qin Wang**, Huawei Technologies Co., Ltd **Speech Title**: All-Domain Collaboration: Kunpeng Computing Bedrock Promotes Domestic EDA Innovation	
14:00-15:40	**Technical Session 20** Advanced Analog Simulation and Verification Techniques	Sleeping Beauty 1/2
	Technical Session 21 Routing, Interconnect, and Partitioning Innovations	Sleeping Beauty 3
	Technical Session 22 Artificial Intelligence in EDA: Library, Innovation and Applications	Sleeping Beauty 5
	Panel 3 The Fusion of AI and Multiphysics: Accelerating EDA Revolution	Snow White 2/3
16:00	**Social Event**	Disneyland Park

May 12, 2025 | Monday		
08:30-09:00	Morning Coffee & Tea	Foyer
Keynote Speech 7 & 8 Host: **Gang Qu**, University of Maryland		Cinderella Ballroom
09:00-09:40	**Prof. Tim Kwang-Ting CHENG**, The Hong Kong University of Science and Technology **Speech Title**: Design and EDA for Edge Inference Chips Supporting Large-Scale Multi-Modal AI Models: The InnoHK ACCESS Approach	
09:40-10:20	**Prof. Sachin S. Sapatnekar**, University of Minnesota **Speech Title**: Automating Analog Design for the 21st Century	
10:20-10:40	Break	Foyer
10:40-12:00	**Technical Session 23** Advanced Timing Analysis and Optimization	Sleeping Beauty 1/2
	Technical Session 24 System-Level Design Exploration and NoC Innovations	Sleeping Beauty 3
	Technical Session 25 RTL and Gate-Level Simulation and Verification	Snow White 2/3
	Technical Session 26 Packaging, Chiplet Design, and Multi-Physics Simulation	Snow White 1
	Technical Session 27 Advanced Simulation and Optimization in Semiconductor Processes	Sleeping Beauty 5
12:00-14:00	Lunch & Keynote Speeches	Cinderella Ballroom
Keynote Speech 9 & 10 Host: **Tsung-Yi Ho**, The Chinese University of Hong Kong		
12:30-13:10	**Prof. Jaijeet Roychowdhury**, University of California, Berkeley **Speech Title**: Oscillator Ising Machines: Principles and Design	
13:10-13:50	**Assoc. Prof. Vijay Janapa Reddi**, Harvard University **Speech Title**: Architecture 2.0: Foundations of Artificial Intelligence Agents for Modern Computer System Design	

KEYNOTE SPEAKERS

09:00-09:40 | May 10, 2025 @ Cinderella Ballroom

Giovanni De Micheli

École polytechnique fédérale de Lausanne (EPFL)

Bio.: Giovanni De Micheli is a research scientist in electronics and computer science. He is credited for the invention of the Network on Chip design automation paradigm and for the creation of algorithms and design tools for Electronic Design Automation (EDA). He is Professor and Director of the Integrated Systems Laboratory and Scientific Director of the EcoCloud center at EPFL Lausanne, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University. He was Director of the Electrical Engineering Institute at EPFL from 2008 to 2019 and program leader of the Swiss Federal Nano-Tera.ch program. He holds a Nuclear Engineer degree (Politecnico di Milano, 1979), a M.S. and a Ph.D. degree in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983).

Prof. De Micheli is a Fellow of ACM, AAAS and IEEE, a member of the Academia Europaea and an International Honorary member of the American Academy of Arts and Sciences. His current research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis for emerging technologies. He is also interested in heterogeneous platform design including electrical components and biosensors, as well as in data processing of biomedical information. He is author of: Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994, co-author and/or co-editor of ten other books and of over 900 technical publications. His citation h-index is above 100 according to Google Scholar. He is member of the Scientific Advisory Board of IMEC (Leuven, B) and STMicroelectronics.

Prof. De Micheli is the recipient of the 2022 ESDA-IEEE/CEDA Phil Kaufman Award, the 2019 ACM/SIGDA Pioneering Achievement Award, and several other awards.

Title: The Future of Computing Systems Design

Abstract: Increasingly more stringent requirements for computing systems will outpace our ability to design them using current technologies and methods. Fortunately, we can leverage design automation tools to analyze and synthesize new generations of computing machines, that will depart from their ancestors in terms of realization technology, computing paradigm and interaction with humans. Devices and chips technologies are already evolving into a third dimension. New materials are both enhancing silicon technology and creating viable alternatives. Accelerators of computation leverage the diversity of underlying technology. Yet their efficient design requires new design automation tools.

Within this plurality of possibilities, the computational intractability of even simple design problems will challenge our goals to achieve both high-performance and low-energy computing. Interestingly, many disparate design problems share kernel subproblems, that can be tackled with the help of graph models and discrete mathematics tools. Synthesis is and will be the key enabler for the progress in computing as well as for addressing efficient ways for enhancing privacy and security.

KEYNOTE SPEAKERS

09:40-10:20 | May 10, 2025 @ Cinderella Ballroom

Georges Gielen

Katholieke Universiteit Leuven (KU Leuven)

Bio.: Georges G.E. Gielen received the MSc and PhD degrees in Electrical Engineering from the Katholieke Universiteit Leuven (KU Leuven), Belgium, in 1986 and 1990, respectively. Currently, he is Full Professor in the MICAS research division at the Department of Electrical Engineering (ESAT) at KU Leuven. From August 2013 until July 2017 he served as Vice-Rector for the Group of Sciences, Engineering and Technology. In 2018 he was visiting professor at UC Berkeley and Stanford University. From 2020 to 2024 he served as Chair of the Department of Electrical Engineering (ESAT) at KU Leuven.

His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation, including modeling, simulation, optimization and synthesis as well as testing.

He is a frequently invited speaker/lecturer and coordinator/partner of several (industrial) research projects in this area, including an ERC Advanced Grant. He has (co-)authored 10 books and more than 700 publications in edited books, international journals and conference proceedings. He is a 1997 Laureate of the Belgian Royal Academy of Sciences, Literature and Arts in the discipline of Engineering. He is Fellow of the IEEE since 2002, and received the IEEE CAS Mac Van Valkenburg award in 2015 and the IEEE CAS Charles Desoer award in 2020, as well as the EDAA Achievement Award in 2021. He is an elected member of the Royal Flemish Academy of Belgium in the class of Technical Sciences, and of the Academia Europaea.

Title: DeepDesignAMS: Will Tomorrow's Analog Integrated Circuits be Generated by AI?

Abstract: Analog/mixed-signal integrated circuits are key in applications where electronics interface with the physical world. But whereas digital circuits are largely synthesized through EDA software, surprisingly, the design of analog circuits in industry is mainly still handcrafted, with long and error-prone design cycles and high development costs. The recent rebirth of AI and machine learning, and the recent rise of generative AI methods, however, create a whole new spectrum of techniques to automate this process. This keynote presentation will explore the high potential of using advanced machine learning (ML) techniques to automatically synthesize and lay out analog integrated circuits. What is hype and what will be feasible? Will we still need analog designers in the future and how will they operate?

KEYNOTE SPEAKERS

12:40-13:20 | May 10, 2025 @ Cinderella Ballroom

Hong Zhou

Institute of Strategic Research, Huawei

Bio.: Dr. Zhou, President of Huawei's Institute of Strategic Research, joined Huawei in 1997. Dr. Zhou has served as Chief of the Shanghai Research Center, Vice President of the Wireless Network Product Line, President of the Central Hardware Engineering Institute, and President of the European Research Institute etc. In these roles, Dr. Zhou has been responsible for research, standardization, industrialization, and technical cooperation activities of the related business.

Title: Building a Better Connected and Intelligent World with STCO Collaborative Development

Abstract: With the rapid development of digitization, intelligence, and greenization, we are standing at an unprecedented node in the era where society and economy, science and technology, culture and education will undergo tremendous changes in the future. This presents both new opportunities and unprecedented challenges for the ICT field, requiring industry and academia to jointly explore future oriented business visions and technological assumptions, from What to Why and How, to develop efficient, and creative intelligence, and build a better connected and intelligent world with STCO Collaborative Development.

09:00-09:40 | May 11, 2025 @ Cinderella Ballroom

Sung Kyu Lim

Georgia Institute of Technology (Gatech)

Bio.: Prof. Sung Kyu Lim earned his Ph.D. in Computer Science from UCLA in 2000. Since 2001, he has been a faculty member at the School of Electrical and Computer Engineering at the Georgia Institute of Technology. His research explores the architecture, design, and electronic design automation (EDA) of 2.5D and 3D integrated circuits, contributing to over 400 published papers. He received the Best Paper Awards from the IEEE Transactions on CAD in 2022 and the ACM Design Automation Conference in 2023. He is an IEEE Fellow and served as a program manager at DARPA's Microsystems Technology Office from 2022 to 2024.

Speech Title: Enhancing AI Chip Design: AI and Traditional Algorithms for Multi-Chip Integration

Abstract: Multi-chip integration has become standard practice in AI training and is increasingly adopted in edge learning applications. By utilizing 2.5D and 3D IC architectures through multi-chip integration, significant improvements can be made in energy efficiency and latency reduction during data transfers. Central to these advancements is the automation of design and simulation processes for heterogeneous AI chips, where sophisticated algorithms increasingly play a pivotal role, rather than manual human intervention. This transition is powered by advanced electronic design automation (EDA) tools. At Georgia Tech, my research team combines AI-driven and conventional algorithms to enhance EDA capabilities, tailored specifically for the development of state-of-the-art heterogeneous AI chips. In my talk, I will highlight these technological innovations and discuss the prevailing challenges in AI chip design and EDA.

KEYNOTE SPEAKERS

09:40-10:20 | May 11, 2025 @ Cinderella Ballroom

Ulf Schlichtmann

Technical University of Munich (TUM)

Bio.: Professor Schlichtmann (b. 1964) explores design automation methodologies for complex (digital and analog) electronic circuits and systems. These often consist of billions of components and need to be designed using sophisticated optimization and analysis algorithms. In recent years, his research has increasingly addressed emerging technologies (photonics, microfluidic biochips, neuromorphic architectures).

Professor Schlichtmann studied electrical engineering at TUM and obtained his doctorate for a thesis on computer-aided design, and also pursued a postgraduate business degree during this time. He then worked for Siemens AG and Infineon Technologies AG in a number of technical, managerial and executive positions for about 10 years. In 2003, Professor Schlichtmann was appointed to a professorship at TUM. In addition to his research and teaching activities, he coordinates international study programs in both Munich and Singapore (TUM Asia). He furthermore serves as program director of the TUMCREATE research project in Singapore and is is a member of various advisory boards and of the acatech National Academy of Science and Engineering.

Title: Optical Networks-on-Chip: EDA for the Future of Interconnect

Abstract: Optical networks-on-chip (ONoC) is a next-generation interconnect architecture, e.g. for multiprocessor systems-on-chip (MPSoC). Compared to classic electrical NoCs, ONoC offers much higher bandwidth with wavelength-division multiplexing (WDM), which allows signals to travel through the same medium simultaneously with little interference by modulating them on different wavelengths. Among various types of ONoCs, Wavelength-Routed ONoC (WRONoC) is renowned for being exempt from communication protocols. Specifically, instead of dynamically constructing/destructing signal paths, optical signals are routed passively according to their wavelengths along designated signal paths fixed in the design phase. This way, WRONoC avoids the energy and latency overhead for arbitration and enables all-to-all simultaneous data transmission. This talk presents three design synthesis methodologies and the corresponding research projects conducted at TUM for application-specific WRONoC. In addition, this talk will highlight opportunities for bit-level parallelism maximization and allocation during and after design synthesis and the corresponding challenges that must be addressed, particularly for large-scale networks.

KEYNOTE SPEAKERS

12:30-13:10| May 11, 2025 @ Cinderella Ballroom

Jinjun Xiong

University at Buffalo

Bio.: Dr. Jinjun Xiong is Empire Innovation Professor with the Department of Computer Science and Engineering at University at Buffalo (UB). He also serves as the Scientific Director for the National AI Institute for Exceptional Education, the AI lead for the IES Center for Early Literacy and Responsible AI, and Director for the SUNY-UB Institute for Artificial Intelligence and Data Science. Prior to that, he was a Senior Researcher and Program Director for AI and Hybrid Clouds Systems at the IBM Thomas J. Watson Research Center. He was the former co-founder and co-director for the IBM-Illinois Center for Cognitive Computing Systems Research (C3SR), the success of which in 5 years has led to the 10-year $200M expansion of the center to the IBM-Illinois Discovery Accelerator Institute. His research interests are on across-stack AI systems research, including AI applications, algorithms, tooling and computer architectures. Many of his research results have been adopted in IBM's products and tools. He published more than 180 peer-reviewed papers in top AI conferences and systems conferences. His publication won 9 Best Paper Awards and 10 Nominations for Best Paper Awards. He also won top awards from various international competitions, including the championship award for the IEEE GraphChallenge on accelerating sparse neural networks in 2020, and the First Place Awards for the 2019 DAC Systems Design Contest on designing an object detection neural network for edge FPGA and GPU devices, respectively.

Title: A Reflection on Machine Learning for EDA: What are Possible Future Directions?

Abstract: The increasing power of deep learning-based machine learning (ML) techniques have started to erode many of the traditional equation-based physical modeling techniques, some of which are corner stone technologies for the development of electronic design automation (EDA) as an active area in the past decades. Since the inception of the new area of ML for EDA, there have always been controversies or doubts on the sensibility of such a formulation. Based on the speaker's years of research experience in both EDA and ML as two separate domains, he will reflect upon his personal learning in these two seemingly different areas, how the controversies may be reconciled, and how a cohesive view on the subject of ML for EDA can be formed. In doing so, the speaker would like to shed some lights on the future of ML for EDA, and what research challenges are ahead of the ML for the EDA research community.

KEYNOTE SPEAKERS

09:00-09:40 | May 12, 2025 @ Cinderella Ballroom

Tim Kwang-Ting CHENG

The Hong Kong University of Science and Technology

Bio.: Professor Tim Cheng is Vice-President for Research and Development (VPRD) and Chair Professor jointly in the Department of Electronic & Computer Engineering (ECE) and Department of Computer Science & Engineering (CSE) at The Hong Kong University of Science and Technology (HKUST). His current research interests span the fields of AI chip design, electronic design automation (EDA), computer vision, and medical image analysis. He is now directing the InnoHK AI Chip Center for Emerging Smart Systems (ACCESS), a multidisciplinary R&D platform aiming to advance IC design and EDA development in realizing ubiquitous AI applications in society.

Prof. Cheng holds a doctorate from the Univ. of California, Berkeley. Prior to joining HKUST, he was on the faculty at the Univ. of California, Santa Barbara (UCSB) after spending five years at the AT&T Bell Laboratories. At UCSB, he took up various academic leadership roles, including the Founding Director of the Computer Engineering Program, Chair of the ECE Department, and Associate Vice Chancellor for Research. He was Dean of Engineering at HKUST from 2016 to April 2022 before becoming VPRD.

A Fellow of IEEE and the Hong Kong Academy of Engineering Sciences, Prof. Cheng has gained due recognition for his research, including a dozen of best paper awards from IEEE and ACM conferences and journals. On top of receiving the UCSB College of Engineering Outstanding Teaching Faculty Award, the 2020 Pan Wen Yuan Outstanding Research Award, and the 2024 CCF Overseas Outstanding Contribution Award, he was named a Fellow of the School of Engineering at the University of Tokyo.

Title: Design and EDA for Edge Inference Chips Supporting Large-Scale Multi-Modal AI Models: The InnoHK ACCESS Approach

Abstract: I will give an overview of the multi-faceted technical approaches and recent results at the InnoHK AI Chip Center for Emerging Smart Systems (ACCESS) research center in designing high-performance and energy-efficient edge accelerators for supporting inference of large-scale AI models. Four major trends are driving ACCESS's research agenda: (1) The growth rate of AI model size and complexity is much faster than the performance improvement rate of AI hardware, (2) latency, scalability, privacy, and reliability are driving migration of AI from cloud to edge, (3) AI model inference market is explosive, becoming much bigger than the model training market, and (4) chiplet/3DIC is going mainstream for AI processor implementation. I will showcase our approaches to design of Transformer and LLM accelerators, compute-in-memory macros, an application-algorithm-architecture co-design framework, and an automatically synthesized FPGA-based accelerator for convex optimization solvers.

KEYNOTE SPEAKERS

09:40-10:20 | May 12, 2025 @ Cinderella Ballroom

Sachin S. Sapatnekar

University of Minnesota

Bio.: Sachin S. Sapatnekar is the Henle Chair in ECE and Distinguished McKnight University Professor at the University of Minnesota. His research interests include design automation methods for analog and digital circuits, circuit reliability, and algorithms and architectures for machine learning and quantum-inspired computing. He is a Fellow of the IEEE and the ACM.

Title: Automating Analog Design for the 21st Century

Abstract: Today's computing models see increasing analog content for two reasons: ever-increasing interaction with an analog real world, and the growing realization that computing on analog substrates can, under certain circumstances, be more efficient than traditional digital computing. For decades, automation has eluded analog design, but with growing design complexity, messy design rules and nontrivial constraints, there has been a renaissance in this field aided partially (but not exclusively) by the emergence of AI. The talk will first overview experience in analog design automation, particularly our experiences with the ALIGN layout automation system, and will overview directions for future research in the field.

12:30-13:10 | May 12, 2025 @ Cinderella Ballroom

Jaijeet Roychowdhury

University of California, Berkeley

Bio.: Jaijeet Roychowdhury is a Professor of EECS at the University of California at Berkeley. His research interests include machine learning, novel computational paradigms, and the analysis, simulation, verification and design of cyber-physical, electronic, biological, nanoscale and mixed-domain systems. Contributions his group has made include the concept of self-sustaining oscillators for Ising-based and von Neumann computation, novel machine-learning techniques for dynamical systems, theory and techniques for oscillator phase macromodels, injection locking and phase noise, multi-time partial differential equations, techniques for model reduction of time-varying and nonlinear systems, and open-source infrastructures for reproducible research.

Roychowdhury received a Bachelor's degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1987, and a Ph.D. degree in electrical engineering and computer science from UC Berkeley in 1993. From 1993 to 1995, he was with the Computer-Aided Design (CAD) Laboratory, AT&T Bell Laboratories, Allentown, PA. From 1995 to 2000, he was with the Communication Sciences Research Division, Bell Laboratories, Murray Hill, NJ. From 2000 to 2001, he was with CeLight Inc. (an optical networking startup), Silver Spring, MD. From 2001-2008, he was with the Electrical and Computer Engineering Department and the Digital Technology Center at the University of Minnesota in Minneapolis.

Roychowdhury was cited for Extraordinary Achievement by Bell Laboratories in 1996 for work on MOS

homotopy. His student Tianshi Wang and he won the Bell Labs Prize in 2019 for their work on Oscillator Ising Machines. Over the years, he has authored or co-authored seven best papers and a distinguished paper. He has served on technical and administrative committees within several conferences and professional organizations, including ICCAD, DAC, DATE, ASP-DAC and CEDA. Roychowdhury was a co-founder of Berkeley Design Automation, a startup later acquired by Mentor Graphics. He is a Fellow of the IEEE.

Title: Oscillator Ising Machines: Principles and Design

Abstract: Modern society has become increasingly reliant on rapid and routine solution of hard discrete optimization problems. Over the past decade, fascinating analog hardware approaches have arisen that combine principles of physics and computer science with optical, electronic and quantum engineering to solve combinatorial optimization problems in new ways---these have come to be known as Ising machines. Such approaches leverage analog dynamics and physics to find good solutions of discrete optimization problems, potentially with advantages over traditional algorithms. Underlying these approaches is the Ising model, a simple but powerful graph formulation with deep historical roots in physics.

About eight years ago, we discovered that networks of analog electronic oscillators can solve Ising problems "naturally". This talk will cover the principles and practical development of these oscillator Ising machines (OIMs). We will touch upon specialized EDA tools for oscillator based systems and note the role of novel nanodevices. Applied to the MU-MIMO detection problem in modern wireless communications, OIMs yield near-optimal symbol-error rates (SERs), improving over the industrial state of the art by 20x for some scenarios.

KEYNOTE SPEAKERS

13:10-13:50 | May 12, 2025 @ Cinderella Ballroom

Vijay Janapa Reddi

Harvard University

Bio.: Vijay Janapa Reddi is an Associate Professor in the John A. Paulson School of Engineering and Applied Sciences at Harvard University. Prior to joining Harvard University, he was an Associate Professor at The University of Texas at Austin. His research interests include computer architecture and runtime systems, specifically in the context of edge and mobile computing systems (smartphones, autonomous vehicles, aerial robots, etc.) to improve their performance, power efficiency, and reliability. Dr. Janapa Reddi is a recipient of multiple honors and technical achievement awards, including the MICRO and HPCA Hall of Fame (2018 and 2019, respectively), the National Academy of Engineering (NAE) Gilbreth Lectureship Honor (2016), IEEE TCCA Young Computer Architect Award (2016), Intel Early Career Award (2013), Google Faculty Research Awards (2012, 2013, 2015, 2017), Best Paper at the 2005 International Symposium on Microarchitecture (MICRO), Best Paper at the 2009 International Symposium on High Performance Computer Architecture (HPCA), and IEEE's Top Picks in Computer Architecture awards (2006, 2010, 2011, 2016, 2017). Beyond his technical research contributions, Dr. Janapa Reddi is passionate about STEM education at early age. He is responsible for the Austin Independent School District's "hands-on" computer science (HaCS) program, which teaches 6th- and 7th-grade students programming and the high-level principles governing a computing system using open-source prototyping platforms like Arudinos. He received a BS in computer engineering from Santa Clara University, an MS in electrical and computer engineering from the University of Colorado at Boulder, and a Ph.D. in computer science from Harvard University.

Speech Title: Architecture 2.0: Foundations of Artificial Intelligence Agents for Modern Computer System Design

Abstract: Modern computing systems have reached unprecedented levels of complexity, rendering traditional design methodologies increasingly inadequate. As system architectures evolve toward greater specialization and heterogeneity, the challenge intensifies, particularly with the rise of domain-specific architectures that demand intricate optimization across multiple design parameters. This complexity explosion necessitates fundamentally new approaches to system design and optimization. Artificial intelligence agents have demonstrated transformative potential across diverse fields, from autonomous systems to scientific discovery, offering data-driven methodologies that can navigate complex decision spaces. These agents, powered by deep learning and reinforcement learning, have shown remarkable capabilities in domains requiring continuous adaptation and intelligent decision-making. The next frontier is to harness similar agent-based approaches for architectural design and optimization, potentially revolutionizing how we approach memory controller optimization, resource allocation, compiler tuning, and power management. While current ML-assisted architecture research has produced innovative algorithms and methods that enhance system efficiency through learned embeddings and automated design space exploration, the full potential of autonomous AI agents in system design remains largely untapped. As we stand at the threshold of "Architecture 2.0," a crucial question emerges: What foundational infrastructure must be established to enable AI agents to transform computer system design? This talk examines the essential building blocks for developing AI agent-assisted architecture research through a shared ecosystem. Such infrastructure would provide standardized environments for agent development, training datasets, and unified platforms for reproducible experimentation and comparative analysis. The talk presents a vision for collaborative ecosystem development that addresses the unique challenges of bringing AI agents to systems and architecture research. Through collective effort, we can establish the foundations to transform modern computer system design for the next generation of computing.

TUTORIALS

T01. Test and Health Monitoring under Approximations and Variations

14:00-17:00 | May 9, 2025 @ Snow White 1

Abstract: Process and dynamic variations including voltage and temperature fluctuations, crosstalk interaction or aging effects complicate distinguishing between defects, reliability threats, and benign behavior. New compute paradigms like approximate computing aggravate the problem since they may hide malicious reliability threats. This tutorial introduces into the most recent techniques for offline and online test and health monitoring under variations and presents simulation and test generation techniques to overcome the multi-dimensional variation space. Case studies show, how error rate monitoring under dynamic voltage/frequency scaling and approximate computing and communication lead to improvements of performance, power consumption and reliability at the same time.

Hans-Joachim Wunderlich

University of Stuttgart

Bio.: Hans-Joachim Wunderlich is Professor Emeritus of the University Stuttgart and a Life Fellow of IEEE. He received the diploma degree in mathematics from the University of Freiburg, Germany, in 1981 and the Dr. rer. nat. (Ph.D. degree) from the University of Karlsruhe in 1986. Since 1991, he has been a full professor. From 2002 to 2018, he was the director of the Institute of Computer Architecture and Computer Engineering at the University of Stuttgart, Germany. He has been associate editor of various international journals and organizer of a variety of IEEE conferences on design, test and fault tolerance of electronic systems. He has published 15 books and book chapters and around 300 reviewed scientific papers in journals and conferences. His research interests include test, reliability, fault tolerance and design automation of microelectronic systems.

TUTORIALS

T02. Advanced Open-Source FPGA HLS and Physical Implementation Tools

14:00-17:00 | May 9, 2025 @ Cinderella 3

Organizers: **Yibo Lin**, Peking University; **Zhi-Xiong Di**, Southwest Jiaotong University

Abstract: Computer-Aided Design (CAD) of Field-Programmable Gate Arrays (FPGAs) has been a hot topic in the rapid advancement and adoption of FPGA technology over the past decades. FPGA CAD flow consists of three major steps: high-level synthesis (HLS) and logic synthesis, physical implementation, and bitstream generation.

FPGA CAD flow has several unique characteristics different from conventional application specific integrated circuit (ASIC) design flows due to the high heterogeneity of FPGA architectures, for example, instance packing, resource heterogeneity and large routing scale. Thus, most of the existing works highly rely on FPGA vendors' CAD tools to obtain indirect feedback and tightly bind to vendors' architectures, limiting the flexibility of algorithms and the ability to adapt to new FPGA architectures.

In this tutorial, we have planned three talks to address different aspects of open-source FPGA CAD tools to tackle those challenges. Our first session will provide OpenPARF, an open-source placement and routing framework for large-scale heterogeneous FPGAs with deep learning toolkits. Our second talk will introduce LEAPS, a comprehensive, systematic, and adaptable multi-die FPGA placement algorithm for SLL minimization. Our third session will delve into novel power modeling and optimization strategies tailored for HLS, and introduce power-efficient design methodologies on modern heterogeneous reconfigurable platform, Versal ACAP.

Zhi-Xiong Di

Southwest Jiaotong University

Bio.: Zhi-Xiong Di, School of Integrated Circuits, Southwest Jiaotong University, Associate Professor, Doctoral Supervisor. His research focuses on physical implementation algorithms, FPGA accelerator design. He has published papers in IEEE TCAS-I, IEEE TCAS-II, IEEE TCAD, DAC, and others. He has served as a Guest Editor for IEEE TCAS-II, and has guided students to win first prizes multiple times in the EDA Elite Challenge.

Zhe Lin

Sun Yat-sen University

Bio.: Zhe Lin is an Assistant Professor at the School of Integrated Circuits, Sun Yat-sen University (SYSU). Before joining SYSU, he held research positions at Peng Cheng Laboratory, where he served as an Associate Research Fellow from January to March 2023 and as an Assistant Research Fellow from March 2020 to December 2021. He earned his Ph.D. in Electronic and Computer Engineering from the Hong Kong University of Science and

Technology (HKUST) in 2020. Dr. Lin was awarded the Huawei Young Academic Talent Funding and Oversea High-Caliber Personnel in Shenzhen. As the first author or corresponding author, his paper has been nominated for best paper awards at ICCD 2024, DATE 2022, and FCCM 2019. He served as a technical program committee member for several leading conferences, such as DAC 2025, DATE 2025, ASP-DAC 2025, and FPT 2024.

Jiarui Wang

Peking University

Bio.: Jiarui Wang is a fourth-year Ph.D. student at the School of Computer Science, Peking University, advised by Prof. Yibo Lin. He received the B.S. degree in Computer Science and Technology from Peking University in 2021. His research focuses are FPGA routing and multi-FPGA system design flows. He has published 11 papers in DAC, ASP-DAC, TCAD and others. He has served as a reviewer for TCAD and TODAES. He is the co-author of OpenPARF, a high-performance open-source FPGA placement and routing framework. He won the first prize of EDA Elite Challenge 2022.

Jing Mai

Peking University

Bio.: Jing Mai is a fourth-year Ph.D. student at the School of Computer Science, Peking University, under the supervision of assistant professor Yibo Lin. He received his bachelor's degree from the School of Information Science and Technology, Peking University in 2021. His research interests include machine learning-assisted electronic design automation, machine learning systems and high performance computing. He has published 13 papers in prestigious venues including DAC, ICCAD, ASP-DAC, ISPD, TCAD, TCAS-I, and TPDS. He is the core author of OpenPARF, a high-performance open-source FPGA placement and routing framework. He led a team to achieve second place in the MLCAD 2023 large-scale FPGA macro placement competition. He received the Best Paper Award at ISEDA 2024 and won First Place in the ACM SIGDA CADathlon Contest 2024.

TUTORIALS

T03. VLSI Physical Design, From 2D to 3D

14:00-17:00 | May 9, 2025 @ Cinderella 2

Organizer: Hailong Yao, University of Science and Technology Beijing

Abstract: VLSI physical design plays a pivotal role in the semiconductor industry. It serves as the crucial bridge between the conceptual design of integrated circuits and their actual fabrication, directly influencing the PPA (power, performance, area) and cost of the final chips. With the relentless pursuit of PPA in modern electronics, the significance of accurate and efficient physical design has become even more pronounced.

In recent years, there has been a remarkable evolution from traditional 2D ICs to 3D ICs. 2D ICs have long been the cornerstone of the semiconductor field, but as the limitations of planar scaling become increasingly evident, 3D IC technology has emerged as a promising alternative. 3D ICs stack multiple layers of active devices vertically, enabling shorter interconnect lengths, higher bandwidth, and better integration of heterogeneous technologies. This transition not only provides new opportunities for innovation, but also poses a series of new challenges in the physical design process.

This tutorial comprehensively covers the entire physical design process for both 2D and 3D ICs. It starts with an in-depth introduction to the fundamental concepts and basic algorithms in physical design, including different floorplanning strategies, placement and routing algorithms, clock tree synthesis methods, and timing analysis techniques. It also explores the latest research results in 3D IC physical design. By the end of this tutorial, attendees will have a solid understanding of the VLSI physical design process, and be acquainted with the challenges and opportunities in the research frontier for both 2D and 3D IC designs.

Hailong Yao

University of Science and Technology Beijing

Bio.: Hailong Yao is a second-level full professor at the School of Computer and Communication Engineering, University of Science and Technology Beijing. He received the Ph.D. degree in computer science and technology from Tsinghua University, Beijing, China, in 2007. From 2007 to 2009, he was a Postdoctoral Research Scholar with the Department of Computer Science and Engineering, University of California at San Diego, La Jolla, CA, USA. He served as Assistant and Associate Professor with the Department of Computer Science and Technology, Tsinghua University from 2009 to 2022. Since 2023, he has been a full Professor with the School of Computer and Communication Engineering, University of Science and Technology Beijing, Beijing, China. His research interests include computer-aided design for ASICs, chiplets, and microfluidic biochips. He has published over 100 academic papers in the EDA field, including more than 20 papers in the CCF-A class TCAD journal and DAC conference. He received several Best Paper Award (Nominations) at ICCAD, SASIMI, GLSVLSI, etc. He was awarded the First Prize for Wu Wenjun Artificial Intelligence Science and Technology Award (Technological Invention Award) in 2022 (the first accomplished person). He serves as the Chair of VLSI Physical Implementation Sub-committee in Ecosystem Development Accelerator of EDA (EDA2) (https://www.eda2.com/), Standing Committee Member of CCF VLSI Design committee. He serves as an

editorial board member of ACM Transactions on Design Automation of Electronic Systems (TODAES), and has served as TPC member of domestic and international conferences in the EDA field (such as DAC, ICCAD, DATE, ASPDAC, ISEDA, etc.) for more than 50 times. He is a senior Member of IEEE.

Yuanqing Cheng

Beihang University

Bio.: Yuanqing Cheng is a tenured associate professor of the School of Integrated Circuit and Engineering, Beihang University, Beijing, China. He received his Ph.D. degree from the Key Laboratory of Computer System and Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China. After one year postdoc study at LIRMM, CNRS, France, he joined Beihang University. His research interests include design automation for 3D integrated circuits, as well as low power and architectural optimization of emerging semiconductor technologies. He is currently an editorial board member of Elsevier Integration, the VLSI journal, TPC member of ICCAD/DATE/ASP-DAC/ISEDA, the Treasury of IEEE CEDA Beijing Chapter and a senior member of the IEEE.

Hao Yan

Southeast University

Bio.: Hao Yan is an Associate Professor at the Southeast University. His research is focused on static timing analysis and optimization. In recent years, he has led projects such as the National Natural Science Fund for Young Scientists, National Key Research and Development Plan, and Provincial Key R&D projects. He has published over 30 papers in the field of Electronic Design Automation (EDA) at conferences such as IEEE/ACM DAC and ICCAD, and received a nomination for the Best Paper at ASP-DAC 2021. He has also guided students to win awards in the Integrated Circuit EDA Design Elite Challenge and the International Timing Analysis Competition (2021&2022 TAU Contest).

TUTORIALS

T04. AHS: An EDA toolbox for Agile Chip Front-end Design

14:00-17:00 | May 9, 2025 @ Sleeping Beauty 3

Organizer: Yun Liang, Peking University

Abstract: Compared to software design, hardware design is more expensive and time-consuming. This is partly because software community has developed a rich set of modern tools to help software programmers to get projects started and iterated easily and quickly. However, the tools are seriously antiquated and lacking for hardware design. Modern digital chips are still designed manually using hardware description language such as Verilog or VHDL, which requires low-level and tedious programming, debugging, and tuning. In this tutorial, we will introduce AHS: AHS: An EDA toolbox for Agile Chip Front-end Design, which covers new hardware design methodologies and various automation tools. From the design perspective, AHS presents different ways that use different programming interfaces and target different scenarios, including 1) a multi-level hardware intermediate representation based high-level synthesis flow, which uses C and C++ as the programming language; 2) an embedded hardware description language, which uses Rust as the programming language. From the verification perspective, we will present agile simulation and debugging tools, which can check the functional and performance behaviors of the hardware. Hardware design determines the peak performance, while the actual performance is determined by the software. In the end, we will also present a compiler and instrumentation tool for the DNN accelerator.

Yun Liang

Peking University

Bio.: Prof Yun (Eric) Liang is currently an Endowed Boya Distinguished Professor in the School of Integrated Circuit and EECS at Peking University. His research interest is at the hardware-software interface with work spanning electronic design automation (EDA), hardware and software co-design, and reconfigurable computing. He has authored over 100 scientific publications in the leading international journals and conferences. His research has been recognized with three Best Paper Awards and six Best Paper Award Nominations. He currently serves as Associate Editor of the ACM Transactions on Embedded Computing Systems (TECS) and ACM Transactions on Reconfigurable Technology and Systems (TRETS). He was the program chair of 30th Annual IEEE International Conference on Application-specific Systems, Architecture and Processors (ASAP) 2019 and the International Conference on Field Programmable Technology (FPT) 2022. He currently serves in the program committees in the premier conferences including DAC, ICCAD, FPGA, FCCM, HPCA, MICRO, ASPDAC, etc.

Jingwen Leng

Shanghai Jiao Tong University

Bio.: Jingwen Leng is a full professor at the Department of Computer Science and Engineering at Shanghai Jiao Tong University. His research direction is the intelligent computer system design for the artificial intelligence, with the focus on performance, energy efficiency, and reliability. He has received multiple grants from National Science Foundation of China and top industrial companies. He has published more than 50 papers in top tier computer architecture conferences and more than 10 domestic/international patents. His work has received best paper award or nomination at venues/conferences including IEEE Micro Top Picks, DAC, and PACT. He was also awarded the DAMO Young Fellow from Alibaba.

TUTORIALS

T05. Formal Verification for EDA

14:00-17:00 | May 9, 2025 @ Sleeping Beauty 5

Organizer: Shaowei Cai, Institute of Software, Chinese Academy of Sciences

Abstract: In the realm of electronic design automation (EDA), the exponential growth in chip complexity-driven by advanced nodes, billions of transistors, and safety-critical applications-demands verification methodologies that transcend traditional simulation. While simulations validate observed scenarios, they cannot exhaustively check all possible states, leaving risks of undetected errors. Formal verification fills this gap, offering exhaustive analysis and becoming indispensable in modern IC development. Two pillars of formal verification-equivalence checking and model checking-play pivotal roles in ensuring functional integrity and reliability.

In this tutorial, we have planned two talks to introduce techniques of equivalence checking and model checking. Our first talk will introduce the fundamentals and recent advancements for constraint solving and combinatorial equivalence checking, with a particular interest in parallel algorithms, noting that constraint solving is the underlying engines for both equivalence checking and model checking. Following this, our second talk will provide an in-depth exploration of model checking, including fundamentals and challenges, as well as some prospects.

Shaowei Cai

Institute of Software, Chinese Academy of Sciences

Bio.: Shaowei Cai is a Professor at Institute of Software, Chinese Academy of Sciences. His research interests include constraint solving and formal verification. He has received the Best Paper Award at SAT 2021 and CP 2024 and Distinguished Paper Award at CAV 2024. He has won 10+ gold medals in SAT competitions, and won the Largest Leading Award and Largest Contribution Award 6 times in SMT Competitions, ranked 1st in more than 20 categories. He has led a team working on EDA formal verification tools, including equivalence checking and model checking. His solvers have been used in several EDA companies and also in software verification industries. The formal tools in his group have been used to successfully identify and fix bugs in XiangShan, which is a high-performance RISC-V multi-core processor.

Hongce Zhang

The Hong Kong University of Science and Technology (Guangzhou)

Bio.: Hongce Zhang is an Assistant Professor in Microelectronics Thrust at Hong Kong University of Science and Technology (Guangzhou). He received his PhD from Princeton University in 2021. He is a co-developer of the Pono model checker and his work on instruction-level abstraction (ILA) received the 2020 ACM TODAES best paper award. He has also served as the chair of IEEE Council on EDA, Guangzhou Chapter in 2023 and the program committee member for DAC, CAV, ICCD, FMCAD, GLSVLSI etc.

TUTORIALS

T06. LLM Applications in EDA

14:00-17:00 | May 9, 2025 @ Sleeping Beauty 1/2

Organizer: Fan Yang, Fudan University

Bei Yu

The Chinese University of Hong Kong

Bio.: Prof. Bei Yu is currently an Associate Professor in the Department of Computer Science and Engineering, The Chinese University of Hong Kong. He has served as TPC Chair of ACM/IEEE Workshop on Machine Learning for CAD, and in many journal editorial boards and conference committees. He received eleven Best Paper Awards from ICCAD 2024 & 2021 & 2013, IEEE TSM 2022, DATE 2022, ASPDAC 2021 & 2012, ICTAI 2019, the VLSI Journal in 2018, ISPD 2017, SPIE Advanced Lithography Conference 2016, and eight ICCAD/ISPD contest awards. He received IEEE CEDA Ernest S. Kuh Early Career Award in 2021, ACM SIGDA Meritorious Service Award in 2022, DAC Under-40 Innovator Award in 2024, and Hong Kong RGC Research Fellowship Scheme (RFS) Award in 2024.

Title: Large Language Model in EDA

Abstract: In this talk, we explore the burgeoning intersection of Large Language Models (LLMs) and Electronic Design Automation (EDA). We critically assess whether LLMs represent a transformative future for EDA or merely a fleeting mirage. By analyzing current advancements, challenges, and potential applications, we dissect how LLMs can revolutionize EDA processes like design, verification, and optimization. Furthermore, we contemplate the ethical implications and feasibility of integrating these models into EDA workflows. Ultimately, this talk aims to provide a comprehensive, evidence-based perspective on the role of LLMs in shaping the future of EDA.

Ying Wang

Institute of Computing Technology, Chinese Academy of Sciences

Bio.: Dr. Ying Wang is an professor in Institute of Computing Technology, Chinese Academy of Sciences, Beijing, and his current research interest includes the chip design automation, reliable computer architecture and memory system. He has published over 100 papers on IEEE/ACM conferences and journals, including TC, DAC, MICRO, HPCA and ICCAD. He has received several awards from international conferences, including the championship of IEEE LPIRC contest at DAC 2016, the championship of the System Design Contest at DAC 2018, 2024 IEEE Top Picks on IC testability and reliability, the Best Paper Award at ITC-Asia, GLSVLSI and ICCD. He is also the recipient of IEEE/ACM DAC under 40 innovator at 2021.

Title: Scaling Up the Hardware Design Capability of LLMs

Abstract: Hardware description language (HDL) code designing is a critical component of the chip design process, requiring substantial engineering and time resources. Recent advancements in large language models (LLMs), such as GPTs, have demonstrated their potential for automate this intricate task. Nevertheless, the

existing LLM-based approaches to HDL code generation do not yet meet the complex requirements of realworld hardware design. Although modern LLMs can process long sequences of context tokens, they often do not produce correspondingly long stretches of code; furthermore, their effectiveness in generating HDL code is still restricted. This tutorial present the AutoSilicon framework, which aims to scale up the hardware design capability of LLMs. AutoSilicon incorporates an agent system, which 1) allows for the decomposition of large-scale, complex code design tasks into smaller, simpler tasks; 2) provides a compilation and simulation environment that enables LLMs to compile and test each piece of code it generates; and 3) introduces a series of optimization strategies. Experimental results show that AutoSilicon could scale the hardware design capability well LLMs in terms of both the design size and quality. To further promote the LLM-based hardware design methodology, we organized the 1st OpenDACs LLM-based Processor Design Competition using the AutoSilicon framework. The outcomes provided a set of lessons learned of LLM-based hardware design methodologies.

Ansuman Banerjee

Advanced Computing and Microelectronics Unit, Indian Statistical Institute

Bio.: Ansuman Banerjee is currently working as a Professor at the Advanced Computing and Microelectronics Unit, Indian Statistical Institute Kolkata since 2010. He received his Bachelor in Engineering from Jadavpur University, and M.S. and Ph.D. degrees from the Indian Institute of Technology Kharagpur -- all in Computer Science. He has an experience of over 20 years working on different projects in Formal Verification for a wide variety of application areas.

Title: Machine Learning and Formal Verification Joining Hands

Abstract: The objective of this talk is to explore the collaborative landscape of Machine Learning (ML) and Formal Verification (FV), both of which are being considered indispensable today in almost all application domains. Recent advances in Machine Learning and Deep Learning (DL), in particular, along with significant advances in hardware architectures, has opened up the possibility of applying learning-based solutions to solve many optimization problems in classical Electronic Design Automation (EDA). In the VLSI design community, Formal Verification is now an established practice. Formal methods can provide rigorous correctness guarantees on hardware designs. Thanks to the availability of mature tools, their use is well established in the industry, and in particular in safety-critical applications as they undergo a stringent certification process. Though apparently, the themes of ML and FV lie in two different dimensions, we believe there is a good scope to integrate these for solving some intriguing research problems. The primary goal of this tutorial is to showcase some of these applications in FV where ML has provided a significant role. The concept of ML for FV foregrounds accelerating the verification process by deploying emerging ML techniques that can come up with fast and scalable automated verification proofs at scale. We talk about our recent work on enhancing the efficiency of the search heuristics inside Bounded Model Checking (BMC) engines that form one of the main backbones of industrial FV today. We discuss how Graph Neural Networks can aid in learning decision points for an integrated verification flow, along with Reinforcement Learning techniques that can help in selection of branching heuristics inside BMC engines. Additionally, we talk about how Large Language Models coupled with Chain-Of-Thought prompting and Retrieval Augmented Generation (RAG) aided with a FV tool in the loop can provide high quality assertions with high coverage. We conclude with a summary of some open challenges in this fascinating domain.

TUTORIALS

T07. AI-Driven Breakthroughs in Next-Generation Circuit Simulation and Reliability

14:00-17:00 | May 9, 2025 @ Snow White 2/3

Organizer: Zhou Jin, Zhejiang University

Abstract: Simulation plays a pivotal role in modern IC design, from transistor-level SPICE analysis to electromigration (EM), IR-drop, and thermal reliability checks. As integrated circuits continue to grow in scale and complexity, driven by advanced 3D integration, simulation and reliability challenges become increasingly intricate. Fast and accurate simulation techniques have thus become indispensable for ensuring performance, reliability, and time-to-market. This tutorial gathers experts from academia and industry to explore cutting-edge AI-driven and advanced simulation methodologies that address these pressing issues.

The first part of the tutorial focuses on LLM-Driven Post-layout Simulation Acceleration, where we demonstrate how large language models (LLMs) can identify parasitic-sensitive nodes in circuits. This information is then used to apply targeted RC reductions in the post-layout simulation phase, significantly accelerating simulation times while maintaining accuracy.

Next, we explore the critical issue of reliability in next-generation ICs with Electromigration-Thermal Co-Simulation. As heterogeneous integration in 3D ICs continues to push the limits of performance, electromigration-thermal coupling has emerged as a major reliability bottleneck. This talk systematically examines the challenges of implementing effective EM-thermal co-simulation methodologies to address these issues.

The final presentation introduces ISPT-Net, a novel approach to transient analysis in large-scale circuits. By leveraging irregular sequential prediction transformers, ISPT-Net provides accurate initial solutions for Newton-Raphson (NR) methods and improves LTE estimation, drastically reducing backward stepping in simulations. This results in significant computational savings and increased accuracy, especially in real-world industrial SPICE simulations.

This tutorial will provide valuable insights into how AI-driven solutions are transforming circuit simulation and reliability analysis, offering attendees a glimpse into the future of automated, high-performance simulation workflows for advanced IC designs.

Zhou Jin

Zhejiang University

Bio.: Prof. Zhou Jin is currently a ZJU100 Young Professor at Zhejiang University. She received her Bachelor's degree from Nanjing University in 2010, followed by her Master's and Ph.D. degrees from Waseda University, Japan, in 2012 and 2015, respectively. From 2017 to 2022, she served as an Assistant Professor at the Super Scientific Software Laboratory, China University of Petroleum, Beijing, and was later promoted to Associate Professor from 2023 to 2024. Her research interests primarily include AI-driven and GPU-accelerated transistor-level nonlinear circuit simulation, as well as hardware-software co-design for linear algebra applications. She has received multiple awards, such as the Best Paper Award at SC'23, Best Paper Award Finalist

at SC'24, Honorable Paper Award at ISEDA'23, and the IEEJ Kyushu Branch Award in 2013, etc.

Speech Title: LLM-Driven Post-Layout Circuit Simulation Acceleration

Abstract: As process nodes advance, post-layout simulations for integrated circuits are becoming increasingly complex, with billions to trillions of nodes. Existing methods for large-scale post-layout circuits face challenges due to high computational costs. In this talk, we introduce PiSPICE, a novel approach that uses adjoint sensitivity analysis to identify and reduce non-critical parasitics, significantly accelerating post-layout simulations. By modeling parasitics and performing sensitivity analysis on pre-layout circuits, PiSPICE reduces computational burden and achieves up to 17.27x speedup with less than 0.78% error compared to Spectre. Additionally, we demonstrate how large language models (LLMs) can be leveraged to directly identify parasitic-sensitive nodes, enabling further RC reduction and speeding up the post-simulation flow.

Zhenya Zhou

Huada Empyrean Technology

Bio.: Mr. Zhenya Zhou is currently a VP of R&D at Huada Empyrean Technology. His research interests include transistor-level circuit simulation, multi-physics analysis, and electromigration (EM) reliability assessment.

Title: Electromigration-Thermal Co-Simulation in 3D ICs: Problems and Challenges

Abstract: As 3D IC technologies push the limits of heterogeneous integration, electromigration-thermal coupling has emerged as a critical reliability bottleneck for advanced nodes. This report systematically examines the problems and challenges in implementing electromigration-thermal co-simulation methodologies.

Dan Niu

Southeast University

Bio.: Dan Niu (Member, IEEE) received the Ph.D. degree from the Graduate School of Information, Production and Systems, Waseda University, Japan. He has been an Associate Professor with the School of Automation, Southeast University, Nanjing, China. His research interests include AI for simulation and verification technologies of large-scale nonlinear circuits and systems, and AI for Spatiotemporal Sequence Prediction.

Title: ISPT-Net: A Noval Transient Backward-stepping Reduction Policy by Irregular Sequential Prediction Transformer

Abstract: In the post-layout simulation for large-scale integrated circuits, transient analysis (TA), determining the timedomain response over a specified time interval, is essential and important. However, it tends to be computationally intensive and quite time-consuming without proper settings of NR initial solution and accurate LTE estimation for determining the next transient timestep, which will lead to a mass of backwardsteppings. In this work, an irregular sequential prediction transformer named ISPT-Net is proposed to predict accurately transient solution as NR initial solution and further obtain precise LTE estimation for setting next timestep. The ISPT-Net is strengthened with timestep positional encoding module (TPE), frequency- and timestep-sensitive muti-head self-attention module (FT-MSA) to enhance irregular sequence feature extraction and prediction accuracy. We assess ISPT-Net in the real largescale industrial circuits on a commercial SPICE simulator, and achieve a remarkable backward stepping reduction: up to 14.43X for NR nonconvergence case and 4.46X for LTE overlimit case while guaranteeing higher solution accuracy.

PANELS

P01. Scaling up AI-Assisted EDA Techniques with Large Foundation AI Models

14:00-15:40 | May 10, 2025 @ Sleeping Beauty 5

Abstract: Artificial intelligence (AI)-driven electronic design automation (EDA) techniques have been extensively explored for VLSI circuit design applications. Most recently, foundation AI models for circuits (e.g., Large Language Models, Large Circuit Models) has emerged as a new technology trend. These models typically leverage a two-stage paradigm of pre-training on large-scale datasets followed by fine-tuning for specific applications, significantly enhancing adaptability across various EDA tasks. Their great potential has attracted wide attention from the EDA community, with representative works being relatively highly cited. In this panel, we invited 6 distinguished researchers with active publications in this field. We will discuss the latest research outputs, existing challenges, and future directions about the development foundation AI models for EDA methodologies.

Key Questions

- **Question 1:** There have been many general LLMs as commercial products, such as GPT or DeepSeek. Do you think foundation AI models (e.g., LLMs) will be adopted in the semiconductor industry as mature products in the near future (5 years)? What are the obstacles in the deployment?
- **Question 2:** Do you think circuit data will limit the development of foundation AI models? How can we solve the data availability problem? Do you think the computation resources will be the limit?
- **Question 3:** Do you think academia or industry will lead this research trend? Will the SOTA foundation circuit models in the future be open-source or in-house?
- **Question 4:** Do you think large foundation models for circuits will replace existing IC design jobs, considering both digital and analog design? Which positions?

Session Chair/Moderator

Zhiyao Xie

The Hong Kong University of Science and Technology

"FOR" Group Speakers

Qiang Xu

The Chinese University of Hong Kong

Bio.: Qiang Xu received his B.E. and M.E. degrees from Beijing University, and his Ph.D. degree from McMaster University. He is a Professor of Computer Science and Engineering, The Chinese University of Hong Kong. His research interests include electronic design automation, trusted computing and representation learning. He is currently serving as an associate editor of IEEE Transactions on Computer-Aided Design and Integrated Circuits and Systems and Integration, the VLSI Journal. He has supervised ~20 Ph.D. dissertations and his students have won EDAA Outstanding Dissertation Award and IEEE TTTC Doctoral Thesis Award.

Cheng Zhuo

Zhejiang University

Bio.: Cheng Zhuo received his B.S. and M.S. from Zhejiang University, Hangzhou, China, in 2005 and 2007. He received his Ph.D. from the University of Michigan, Ann Arbor, in 2010. He is currently Qiushi Distinguished Professor at Zhejiang University with research focus on hardware intelligence, machine learning-assisted EDA, and low power designs. He has published over 200 technical papers and received 4 Best Paper Awards, 6 Best Paper Nominations, and 2 international design contest awards. He is also the recipient of ACM/SIGDA Meritorious Service Award and Technical Leadership Award, JSPS Faculty Invitation Fellowship, Humboldt Research Fellowship, etc. He has served on the organization/technical program committees of many international conferences, as the area editor for Journal of CAD&CG, and as Associate Editor for IEEE TCAD, ACM TODAES, and Elsevier Integration. He is IEEE CEDA Distinguished Lecturer, a senior member of IEEE, and a Fellow of IET.

Fan Yang

Fudan University

Bio.: Fan Yang received the B.S. degree from Xi'an Jiaotong University, Xi'an, China, in 2003, and the Ph.D. degree from Fudan University, Shanghai, China, in 2008. He is currently a Full Professor with the Microelectronics Department, Fudan University. His research interests include model order reduction, circuit simulation, high-level synthesis, acceleration of artificial neural networks, and yield analysis and design for manufacturability. He won First-class prize of Natural Science Shanghai in 2012, Best Paper award of Integration, the VLSI Journal 2018, First Place of ICCAD contest 2022 Problem C. He also got several best paper nominations such as DAC 2014, DAC 2017 and ASPDAC 2017. He was supported by National Science Foundation for Excellent Young Scholars in 2018.

Huawei Li

Institute of Computing Technology, Chinese Academy of Sciences

Bio.: Huawei Li received the B.S. degree in computer science from Xiangtan University, Xiangtan, China, in 1996, and the M.S. and Ph.D. degrees from the Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS), Beijing, China, in 1999 and 2001, respectively. She has been a Professor with the ICT, CAS, since 2008. She has also been with the School of Computer Science and Technology, University of Chinese Academy of Sciences, Beijing, since 2012. She was a Visiting Professor with the University of California at Santa Barbara, Santa Barbara, CA, USA, from 2009 to 2010. Her current research interests include testing of VLSI/SoC circuits and error tolerant computing. Prof. Li currently serves as an Associate Editor for the IEEE TRANSACTION ON VLSI SYSTEMS and IEEE DESIGN & TEST.

"AGAINST" Group Speakers

Yun Liang

Peking University

Bio.: Yun Liang is an Endowed Boya Distinguished Professor in the School of Integrated Circuit and School of EECS at Peking University. His research interest is at the hardware-software interface with work spanning electronic design automation (EDA), hardware and software co-design, and computer architecture. His recent publications investigate new algorithms, programming models, design automation tools and methodologies, and hardware for high-performance and energy-efficient computer systems. He has authored over 100 scientific publications in the leading international journals and conferences. His research has been recognized with four Best Paper Awards, six Best Paper Award Nominations, National Science Fund for Distinguished Young Scholars, CCF-IEEE CS Young Computer Scientist Award, Beijing Natural Science Fund for Distinguished Young Scholars, Beijing Academy of Artificial Intelligence (BAAI) Young Scientist Award, and National Youth Top-notch Talent Fund. He is an ACM Distinguished Scientist/Member and received the Teaching Excellence Award Peking University in 2024. He currently serves as Associate Editor of the ACM Transactions on Embedded Computing Systems (TECS) and ACM Transactions on Reconfigurable Technology and Systems (TRETS). He was the program chair of ASAP 2019 and FPT 2022.

Mingxuan Yuan

Huawei Noah's Ark Lab

Bio.: Mingxuan Yuan received the Ph.D. degree in computer science and engineering from Hong Kong University of Science and Technology, Hong Kong, in 2012. He is currently a Principal Researcher with Huawei Noah's Ark Lab, Hong Kong. He has more than 11 years of industrial research experience and has led several research projects, including spatiotemporal data analysis, telecommunication data mining, enterprise intelligence, and AI4EDA. His research interests include learning to optimize, AI solvers, and data-driven EDA algorithms.

PANELS

P02. AI/LLM for IC Manufacturing

16:00-18:00 | May 10, 2025 @ Sleeping Beauty 5

Abstract: Integrating Large Language Models (LLMs) into IC manufacturing represents a transformative shift in how semiconductor processes are optimized, analyzed, and automated. LLMs have the potential to bridge knowledge gaps, accelerate design-to-manufacturing workflows, and enhance decision-making across DFM, TCAD, and Lithography. However, challenges remain in their trustworthiness, adaptability, and integration with existing workflows. This panel will bring together leading experts from academia and industry to explore where and how LLMs can bring real value to IC manufacturing, the technical and industrial barriers to adoption, and the long-term implications for semiconductor process optimization, cost reduction, and innovation acceleration. Through this discussion, we aim to uncover whether LLMs will merely serve as a complementary tool or drive a paradigm shift in how IC manufacturing is approached in the AI era.

Key Questions

- **Question 1:** Which areas of IC manufacturing can LLMs fundamentally transform, and where will their impact be most significant?
- **Question 2:** What are the key technical and practical challenges in applying LLMs to IC manufacturing, and how can they be addressed?
- **Question 3:** What unique opportunities do LLMs create for enhancing efficiency, collaboration, and knowledge transfer in semiconductor manufacturing?
- **Question 4:** How can LLMs be integrated with traditional AI/ML and physics-based simulation methods to achieve the best results?
- **Question 5:** What are the risks of relying on LLMs in a manufacturing process, and how can the industry mitigate them?
- **Question 6:** Will LLMs lead to a fundamental shift in IC manufacturing, or will they remain a supporting tool for existing methodologies?

Session Chair/Moderator

Qi Sun

Zhejiang University

"FOR" Group Speakers

Lan Chen

Institute of Microelectronics, Chinese Academy of Sciences

Bio.: Dr. Lan Chen, Professor of UCAS and Institute of Microelectronics CAS. Professor Lan Chen got her Ph.D degree from Institute of Computing Technologies, CAS, the research area is advanced computer architecture She is the director of the Beijing Key Laboratory of Three dimensional and nanoscale integrated circuit design automation technologies. She is the fellow of SMIC industry-academic Joint research Center, and Consulting Member of Hupan research Lab of DAMoYuan Alibaba corp(2021-..) She is also the honor of Special government allowances of the State Council, the National Prize for Progress in Science and Technology and the Outstanding Scientific and Technological Achievement Prize of the Chinese Academy of Sciences. The main research area of Dr. Chen includes IC design methodology and EDA, EDA technologies with deep learning, AIoT architecture and processor, hardware security et al. Dr. Chen proposed a set of CMP modeling technologies with Multiphysics and machine learning technologies, and developed a set of DFM toolkits which can predict the manufacture hotspots and accuracy timing analysis, which have verified by industry. She has owned more than 100 patents including 4 PCT, and has published more than 90 research papers.

Qi Sun

Zhejiang University

Bio.: Qi SUN is a ZJU100 Young Professor at the College of Integrated Circuits, Zhejiang University. Before joining ZJU, he worked with Prof. Zhiru Zhang as a Post-Doctoral Associate at the School of Electrical and Computer Engineering, Cornell University. Previously, he received his Ph.D. degree from the Dept. of CSE, CUHK, under the supervision of Prof. Bei Yu in Jul. 2022. His research interests include ML in EDA, design space exploration, RISC-V SoC, and LLM for DTCO. His work has been recognized with two ICCAD Best Paper Awards (top tier EDA conference), Bronze Medal of the ICCAD Student Research Competition, and a Best Paper Award Nomination of DATE.

Xiaoming Liu

Beijing Empyrean Co., Ltd.

Bio.: Product Director at Beijing Empyrean Co., Ltd., with over 10 years of experience in ASIC chip design, manufacturing, and EDA software development and management. He specializes in the planning, development, and promotion of EDA products, having built a comprehensive analog EDA flow solution that has expanded into a wide range of analog chip design domains, including flat panel displays, signal chains, memory, RF, and optoelectronics. He is currently leading the development of a PPAC-driven co-design solution that integrates design, manufacturing, and packaging. Many of the products under his leadership have been adopted into the standard design flows of leading IC design companies both in China and internationally, earning high recognition across the industry.

"AGAINST" Group Speakers

Hao Geng

ShanghaiTech University

Bio.: Prof. Hao GENG is an assistant professor at ShanghaiTech University (ShanghaiTech). Prior to that, he got Ph.D. in Computer Science and Engineering from The Chinese University of Hong Kong (CUHK) in 2021. Previously, he received M.Sc. with Merit from Department of Computing, Imperial College London in 2016, and M.Eng. from USTC in 2015. His research interests include machine learning, deep learning, and optimization methods with applications in EDA, especially design space exploration and computational lithography.

Mingxuan Yuan

Huawei Noah's Ark Lab

Bio.: Mingxuan Yuan is currently a principal researcher and the director of applied AI model projects of Huawei Noah's Ark Lab. Before joining Huawei, he worked in HKUST as a post-doc researcher. He obtained his Ph.D degree from the Hong Kong University of Science and Technology. He has more than 12 years industrial research experience and has led several research projects including telecommunication data mining, enterprise intelligent, AI Solver, AI4EDA and to Business AI models. His research interests include data-driven optimization algorithms, data-driven SAT/MIP solving algorithms, data-driven EDA algorithms and applied large model techniques.

Xingsheng Wang

Huazhong University of Science and Technology

Bio.: Xingsheng Wang is a professor at the School of Integrated Circuits, Huazhong University of Science and Technology (HUST), China. He obtained his Master degree from Tsinghua University and PhD degree from the University of Glasgow, UK (as received the UK ORSAS Award) in 2007 and 2010, respectively. He worked for Synopsys as senior engineer, and he returned to China and became a professor of HUST in February 2018. He received provincial and national talent program projects. He is mainly engaged in the research of novel memories and compute-in-memory integrated chip technology, design technology co-optimization (DTCO) methodology. He has been in charge of the key projects of the National Natural Science Foundation of China and the National Key Research and Development Programme of China. He has published more than 120 papers in journals and conferences, including IEEE EDL, TED, TVLSI, and DAC. He received Huawei OlympusMons Pioneer Awards 2022.

PANELS

P03. The Fusion of AI and Multiphysics: Accelerating EDA Revolution

14:00-15:40 | May 11, 2025 @ Snow White 2/3

Abstract: As semiconductor technology advances, multiphysics challenges-spanning thermal, electromagnetic, semiconductor physics and beyond—have become increasingly complex and computationally demanding. Traditional simulation and modeling techniques often struggle to balance accuracy, efficiency, and scalability, creating a pressing need for innovative approaches. AI has emerged as a powerful tool to revolutionize multiphysics analysis, enabling faster, more efficient, and intelligent solutions in EDA. This panel will bring together leading scholars and industry experts to discuss how AI is transforming multiphysics analysis in EDA. Topics will include AI-accelerated simulation, machine learning-based surrogate modeling, and physics-informed neural networks. The panelists will also explore the challenges of incorporating AI into existing design flows and its impact on design accuracy, efficiency, and manufacturability.

Key Questions

- **Question 1:** Can AI accelerate multiphysics simulations without compromising accuracy, reliability, or verification standards?
- **Question 2:** Which is the more promising direction: integrating AI into physics-based modeling, or embedding physics principles into AI architectures?
- **Question 3:** Can data-driven methods eventually earn enough trust to replace physics-based solvers in critical stages like design sign-off?

Session Chair/Moderator

Quan Chen

Southern University of Science and Technology

"FOR" Group Speakers

Zhou Jin

Zhejiang University

Bio.: Zhou Jin is currently a ZJU100 Young Professor at Zhejiang University. She received her Bachelor's degree from Nanjing University in 2010, followed by her Master's and Ph.D. degrees from Waseda University, Japan, in 2012 and 2015, respectively. From 2017 to 2022, she served as an Assistant Professor at the Super Scientific Software Laboratory, China University of Petroleum, Beijing, and was later promoted to Associate Professor from 2023 to 2024. Her research interests primarily include AI-driven and GPU-accelerated transistor-level nonlinear circuit simulation, as well as hardware-software co-design for linear algebra applications. She has received multiple awards, such as the Best Paper Award at SC'23, Best Paper Award Finalist at SC'24, Honorable Paper Award at ISEDA'23, and the IEEJ Kyushu Branch Award in 2013, etc.

Qinzhi Xu

Institute of Microelectronics, Chinese Academy of Sciences

Bio.: Qinzhi Xu is currently a professor and doctoral supervisor in Institute of Microelectronics of the Chinese Academy of Sciences. His main research interests focus on multiphysics modeling and software development of heterogeneous integration systems, theories and modeling simulators of chemical mechanical planarization, design for manufacturability in nano-scale integrated circuits and development of models and simulation tools for predicting the structure and properties of polymeric materials. He has undertaken more than 20 National, Beijing City, Chinese Academy of Sciences and Enterprise projects, published over 40 modeling papers in interdisciplinary fields of integrated circuits, EDA, polymer nanocomposites, and computational chemistry as the first or corresponding author, applied for nearly 50 patents as the first inventor and obtained several software copyrights of chiplet simulation. He also has received the Third Prize of Beijing Science and Technology Award and the Second Prize of Science and Technology Award of the Chinese Institute of Electronics.

Ting-Jung Lin

Ningbo Institute of Digital Twin, Eastern Institute of Technology

Bio.: Dr Lin is currently an associate research fellow at Ningbo Institute of Digital Twin, Eastern Institute of Technology. She is also a core member of the Engineering Research Center of Chiplet Design and Manufacturing of Zhejiang Province and an R&D director of BTD Technology Co., Ltd. She received her PhD from Princeton University in 2014 and worked with Synopsys' verification group from 2014 to 2017. Her research interests include AI-driven circuit design automation and characterization. Dr. Lin has multiple publications in top EDA conferences including DAC and ICCAD, and journals such as IEEE TVLSI. She has received several best paper awards from international conferences such as ISLAD'24 and ISEDA'24.

"AGAINST" Group Speakers

Xingsheng Wang

Huazhong University of Science and Technology

Bio.: Xingsheng Wang is a professor at the School of Integrated Circuits, Huazhong University of Science and Technology (HUST), China. He obtained his Master degree from Tsinghua University and PhD degree from the University of Glasgow, UK (as received the UK ORSAS Award) in 2007 and 2010, respectively. He worked for Synopsys as senior engineer, and he returned to China and became a professor of HUST in February 2018. He received provincial and national talent program projects. He is mainly engaged in the research of novel memories and compute-in-memory integrated chip technology, design technology co-optimization (DTCO) methodology. He has been in charge of the key projects of the National Natural Science Foundation of China

and the National Key Research and Development Programme of China. He has published more than 120 papers in journals and conferences, including IEEE EDL, TED, TVLSI, and DAC. He received Huawei OlympusMons Pioneer Awards 2022.

Pinghao Jia

Hubei NineCube Microelectronics Co., Ltd.

Bio.: Pinghao Jia is currently the Finite Element Product Chief Architect and Solver Development Team Lead at Hubei Jiu Tongfang Microelectronics Co., Ltd. In this leadership role, he oversees the architectural design of EM simulation software and directs solver development initiatives. He received the B.S. and Ph.D. degrees in electromagnetic field and microwave technology from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2012 and 2019, respectively. From 2018 to 2019, he was a Visiting Scholar with the Department of Electrical and Computer Engineering, Duke University. Dr. Jia later transitioned to industry as a Senior Algorithm Engineer at Huawei Technologies (Shanghai, 2020-2023), where he applied cutting-edge computational electromagnetic techniques to solve complex real-world engineering challenges. Dr. Jia made outstanding contributions to electromagnetic algorithms, earning him the prestigious First Prize of China Electronics Society Science and Technology Award in 2022. His research interests include Electromagnetic simulation software architecture, High-performance solver development, Finite element method (FEM) and integral equation methods (MoM) applications in EM, Algorithm optimization for EM simulation.

SPECIAL SESSIONS

SS01. CEDA-adjoint Special Session: Deep Learning Inspired Algorithms for Physical Modeling and Analysis of Advanced IC Design

14:00-15:40 | May 10, 2025 @ Snow White 3

Organizer/Chair(s)

Yuanqing Cheng

Beihang University

Wenjian Yu

Tsinghua University

Invited Talks

Yibo Lin

Peking University

Bio.: Yibo Lin is an assistant professor in the School of Integrated Circuits at Peking University. He received the B.S. degree in microelectronics from Shanghai Jiaotong University in 2013, and his Ph.D. degree from the Electrical and Computer Engineering Department of the University of Texas at Austin in 2018. His research interests include physical design, machine learning applications, and GPU/FPGA acceleration. He has received multiple Best Paper Awards at premier venues including DATE 2023, DATE 2022, TCAD 2021, and DAC 2019. He has also served in the Technical Program Committees of many major conferences, including ICCAD, ICCD, ISPD, and DAC.

Title: Deep Learning Inspired Thermal-aware Modeling and Optimization for Chiplet Systems

Abstract: Chiplet systems promise enhanced performance but face thermal design challenges. This talk explores deep learning solutions for thermal-aware modeling and optimization. We cover cross-stage power prediction using graph neural networks, physics-based compact thermal models for efficient simulation, novel algorithms for stable transient thermal prediction, and thermal-aware chiplet placement optimization that balances wirelength and temperature. These approaches address nonlinearity and scalability while achieving significant speedups over traditional methods. Experimental results demonstrate their impact on thermal management and design efficiency, paving the way for optimized chiplet integration.

Zhou Jin

Zhejiang University

Bio.: Zhou Jin is currently a ZJU100 Young Professor at Zhejiang University. She received her Bachelor's degree from Nanjing University in 2010, followed by her Master's and Ph.D. degrees from Waseda University, Japan, in 2012 and 2015, respectively. From 2017 to 2022, she served as an Assistant Professor at the Super Scientific Software Laboratory, China University of Petroleum, Beijing, and was later promoted to Associate Professor from 2023 to 2024. Her research interests primarily include AI-driven and GPU-accelerated transistor-level

nonlinear circuit simulation, as well as hardware-software co-design for linear algebra applications. She has received multiple awards, such as the Best Paper Award at SC'23, Best Paper Award Finalist at SC'24, Honorable Paper Award at ISEDA'23, and the IEEJ Kyushu Branch Award in 2013, etc.

Title: G-SpNN: GPU-Accelerated Passivity Enforcement for S-Parameter Macromodeling with Neural Networks

Abstract: The increasing complexity of high-frequency circuits calls for efficient and accurate passive macromodeling techniques. Existing passivity enforcement methods, including those in com- mercial tools, often encounter convergence issues or compromise accuracy. The Domain-Alternated Optimization (DAO) framework seeks to restore accuracy through an additional optimization step but is hampered by high memory consumption and slow convergence, particularly for large-scale problems. This talk introduces G-SpNN, a novel GPU-accelerated framework that recasts the passivity-enforced macromodeling problem as a neural network training task. This approach significantly enhances both the speed and scalability of passivity enforcement. Experimental results show that G-SpNN achieves an average speedup of 7.63× in convergence compared to DAO, while reducing memory usage by two orders of magnitude. This enables G-SpNN to handle complex, high-port-count circuits with greater accuracy and efficiency, paving the way for robust high-frequency circuit simulations.

Yuanqing Cheng

Beihang University

Bio.: Yuanqing Cheng is an associate professor of the School of Integrated Circuit and Engineering, Beihang University, Beijing, China. He received his Ph.D. degree from the Key Laboratory of Computer System and Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China. After one year postdoc study at LIRMM, CNRS, France, he joined Beihang University. His research interests include design automation for 3D integrated circuits, as well as low power and architectural optimization of emerging semiconductor technologies. He has published more than 50 papers including top ranked journals and conferences such as PIEEE, DAC, ICCAD TCAD and TVLSI. He is currently an editorial board member of Elsevier Integration, the VLSI journal, TPC member of ICCAD/DATE/ASP-DAC/ISEDA, the Treasury of IEEE CEDA Beijing Chapter and a senior member of the IEEE.

Title: Machine Learning for Multi-corner Timing Analysis

Abstract: Static Timing Analysis (STA) is an essential and crucial part in the design of modern advanced nanoscale integrated circuits. However, with the continuous increase in the number of process corners, performing STA at each physical design stage has become extremely time-consuming. To address this challenge, we first propose a multi-process-corner and multi-stage timing analysis prediction framework based on a latent feature Bayesian model, achieving a high-precision timing prediction. Furthermore, we optimized it to obtain the ASAP model. By integrating the latest deep learning technology with the classical Bayesian model and using the combination of self-attention mechanism and neural processes, it provides faster and more accurate predictions. In addition, to further reduce the number of required dominant corners, we first propose a neural network matrix completion method named MCSTA based on point-by-point filling, which provides a technical basis for predicting a large number of unknown timing data from a small amount of known timing data. Then we further optimized it to get the LIA (Less Instead of Many) method, which updates the

point-by-point filling method to a method for predicting with an extremely small number of dominant corners. The algorithm adopts a dual-neural-network architecture based on matrix completion to capture the correlation between timing paths and process corners. It successfully reduces the number of required dominant corners to 2-3, and the runtime overhead is reduced by several orders of magnitude.

Wenjian Yu

Tsinghua University

Bio.: Dr. Wenjian Yu is a Full Professor with the Department of Computer Science and Technology, Tsinghua University, Beijing, China. His current research interests include physical-level modeling and simulation techniques for IC design, high-performance numerical algorithms, and big-data analytics. Dr. Yu has coauthored four books and over 200 papers in refereed journals and conferences. He was the recipient of the distinguished Ph.D. Award from Tsinghua University in 2004, the Excellent Young Scholar from NSFC in 2014, and the 2nd-Class Science and Technology Award from CCF in 2022. He received the Best Paper Awards of DATE'2016, ACES'2017 and ICTAI'2019, and 8 Best Paper Award Nominations on prominent EDA conferences including ICCAD, DATE, ASPDAC, GLSVLSI and ISQED.

Shan Shen (Online)

Nanjing University of Science and Technology

Bio.: Shan Shen, male, associate professor of the School of Microelectronics. His main research direction is large-scale circuit simulation technology based on machine learning and SRAM circuit design. He has published 14 papers so far, including 8 papers as the first author. Many of his first-author research results have been published in top academic conferences and journals such as TCAD, DAC, DATE, TCAS, and TVLSI. He is also a member of the DAC Technical Program Committee. His research interests include machine learning, large-scale circuit fast simulation methods, memory circuit design, low-power circuit design, etc.

Title: Pre-layout Prediction of Parasitic Parameters in AMS Circuits Based on Graph Neural Networks

Abstract: Graph representation learning is a powerful method to extract features from graph-structured data, such as analog/mixed-signal (AMS) circuits. However, training deep learning models for AMS designs is severely limited by the scarcity of integrated circuit design data. In this work, we present CircuitGPS, a few-shot learning method for parasitic effect prediction in AMS circuits. The circuit netlist is represented as a heterogeneous graph, with the coupling capacitance modeled as a link. CircuitGPS is pre-trained on link prediction and fine-tuned on edge regression. The proposed method starts with a small-hop sampling technique that converts a link or a node into a subgraph. Then, the subgraph embeddings are learned with a hybrid graph Transformer. Additionally, CircuitGPS integrates a low-cost positional encoding that summarizes the positional and structural information of the sampled subgraph. Our method demonstrates strong inherent scalability, enabling direct application to diverse AMS circuit designs through zero-shot learning. Furthermore, the ablation studies provide valuable insights into graph models for representation learning.

SPECIAL SESSIONS

SS02. Bridging AI and Hardware: Advancing Specialized Circuits, Design Automation, and Manufacturing

16:00-18:00 | May 10, 2025 @ Sleeping Beauty 3

Motivation: Advances in semiconductor design and manufacturing are being driven by a convergence of artificial intelligence (AI) and novel hardware techniques, fueling unprecedented efficiency and innovation. Bridging the gap among chip manufacturing, edge deployment, and circuit design optimization has become essential for tackling the rising complexity and scalability demands of today's systems. As technology node shrinks and application proliferates, balancing performance, cost, and reliability requires cross-layer solutions from fabrication to system-level automation.

This two-hour special session features four invited talks addressing these cross-cutting challenges. It begins with the design of a flexibly configurable, high-performance random number source specifically tailored for stochastic computing, highlighting crucial advancements in circuit design and configurability for new-generation AI hardware. The second talk presents a roadmap for design automation with machine learning, envisioning methodology advancements from supervised learning to foundation models targeting semi- and non-supervised learning scenarios. The third talk explores how large language model (LLM)-based foundation models revolutionize hardware design automation, reducing manual intervention in complex workflows and enabling efficient logic optimization, RTL synthesis, and layout generation. Finally, the session concludes with the deployment of edge-optimized LLMs for real-time anomaly detection in chip manufacturing, addressing latency, privacy constraints, and model adaptability in dynamic production environments.

Together, these presentations highlight how innovative tools and methodologies are revolutionizing both the development and deployment of semiconductor technologies. By fostering synergies across manufacturing intelligence, edge computing, and design automation, this session aims to inspire researchers and practitioners to reimagine chip design and manufacturing, and accelerate the development of scalable, robust, and high-performance semiconductor solutions.

Organizer/Chair(s)

Weikang Qian

Shanghai Jiao Tong University

Zheyu Yan

Zhejiang University

Invited Talks

Kuncai Zhong

Hunan University

Bio.: Kuncai Zhong is currently an Assistant Professor and Ph.D. Supervisor at the School of Semiconductor (School of Integrated Circuits), Hunan University. He received his Ph.D. through the Direct Doctoral Program from the University of Michigan-Shanghai Jiao Tong University Joint Institute in 2024, supervised by Prof. Weikang Qian, and his B.S. degree from the School of Electronic and Information Engineering, Xi'an Jiaotong

University. His research focuses on high-energy-efficiency and secure computing circuit design through computer-aided approaches and trusted root architecture optimization. He has published over 10 papers in top-tier EDA conferences (e.g., DAC, ICCAD, DATE) and holds two national patents as the first inventor. He leads a Key Project of the Changsha Natural Science Foundation and serves as the Program Chair of ITC-Asia 2024 (a CCF-C conference). His contributions as a reviewer span multiple IEEE journals (TCAD, TCAS-I, TVLSI) and conferences (ISCAS, GLVLSI). He was awarded the Second Prize in the 2024 China Graduate EDA Elite Challenge (as first instructor) and the Second Prize in Hunan University's 2023 Teaching Competition for New Faculty. His work bridges innovative circuit design methodologies with industrial applications in semiconductor technologies.

Title: Accuracy Analysis and Design Optimization for Low-Cost High-Accuracy Stochastic Circuit

Abstract: Stochastic computing (SC) performs arithmetic operations using values encoded as stochastic bit streams, enabling low-cost circuitry with inherent fault tolerance. As a promising approach for the post-Moore era, SC faces three key challenges: time-consuming accuracy verification, area-intensive randomizers, and suboptimal component-level optimization. To address these issues, this work presents five technical contributions. First, an analytical accuracy evaluation method enables 765× faster verification than the Monte Carlo simulation for DFF-based SC circuits. Second, an optimized RNS architecture reduces randomizer area by 88% while maintaining equivalent accuracy in general SC designs. Third, for univariate functions, a compact SNG/DFF architecture with scrambling techniques achieves 76% area reduction. Fourth, FIR filter implementations benefit from specialized PCC optimizations, handling both variable and constant probabilities. Finally, a co-optimization framework coordinates randomizers and SC cores to reduce area by 39.7% and power by 42.74%. Experimental results demonstrate consistent improvements in area-accuracy efficiency across all evaluated applications.

Zhiyao Xie

The Hong Kong University of Science and Technology

Bio.: Zhiyao Xie is an Assistant Professor in ECE at HKUST, specializing in electronic design automation (EDA) and AI for chip design. He earned his Ph.D. from Duke University (2022) under Profs. Yiran Chen and Hai Li, following a B.Eng with first-class honors from CityU HK (2017). During his Ph.D., he interned at NVIDIA, Arm, Cadence, and Synopsys. He was awarded the RGC HK Early Career Award 2023 (top 7/525), ACM & EDAA Outstanding Dissertation Awards 2023, and MICRO 2021 and ASP-DAC 2023 Best Paper Awards, he also received the HKUST Faculty Teaching Excellence Appreciation Award (2023/24). His honors include the WAIC Yufan Award and multiple best paper nominations. He serves as TPC member for DAC, ICCAD, DATE, and others, and reviews for leading journals like IEEE TCAD and ACM TODAES. He is the Finance Chair of IEEE CEDA Hong Kong.

Title: AI-Assisted EDA: from Supervised Learning to Circuit Foundation Models

Abstract: As the integrated circuit (IC) complexity keeps increasing, the chip design cost is skyrocketing. There is a compelling need for design efficiency improvement through new electronic design automation (EDA) techniques. As a result, AI-driven EDA techniques have been extensively explored for VLSI circuit design applications. In this talk, I will present the recent trend of developing foundation AI models for circuit design, also named circuit foundation models (CFMs). I will categorize existing circuit foundation models into two

primary types: 1) encoder-based methods for general circuit representation learning for predictive tasks; and 2) decoder-based methods leveraging large language models (LLMs) for generative tasks. I will introduce representative works in each category, as well as our observed challenges and potential future research directions.

Zhenge Jia

Shandong University

Bio.: Zhenge Jia is currently a "Qilu Young Scholar" Professor at the School of Computer Science and Technology, Shandong University. He was also selected as a Young Expert of the Taishan Scholars of Shandong Province. Before joining SDU, he was a Postdoctoral Research Associate at the University of Notre Dame from 2022 to 2024, supervised by Prof. Yiyu Shi. He obtained his Ph.D. degree from the University of Pittsburgh in 2022, supervised by Prof. Jingtong Hu. He earned his B.S. degree (Honors) in Advanced Computing from the Australian National University in 2017, supervised by Prof. Weifa Liang. His research interests include embedded AI and personalized learning.

Title: LLM for Hardware Design: Accelerating Automation with Large Language Models

Abstract: As semiconductor design complexity escalates, leveraging large language models (LLMs) to automate hardware design processes has emerged as a pivotal innovation for overcoming traditional bottlenecks. This talk explores the transformative potential of LLMs in accelerating hardware design workflows, from architectural exploration to layout synthesis. We present a systematic analysis of current LLM-driven approaches to hardware design automation, categorizing them by their application functions, such as logic optimization, RTL generation, and design scoring. Additionally, we discuss methodologies for enhancing LLM adaptability in practical RTL design synthesis. Finally, we outline future research directions, emphasizing the integration of LLMs with physics-aware frameworks and collaborative human-AI design paradigms. This study aims to inspire novel solutions that harness LLMs to bridge the efficiency gap in next-generation hardware design, enabling faster innovation cycles in the era of advanced technology nodes.

Zheyu Yan

Zhejiang University

Bio.: Zheyu Yan is currently an Assistant Professor (ZJUY100 Young Professor) at the College of Integrated Circuits, Zhejiang University. Before joining ZJU, he received his Ph.D. from the University of Notre Dame in 2024 and his B.S. from Zhejiang University, Hangzhou, China, in 2019. His general research direction is hardware/software co-design for neural network accelerators. His current interests include ondevice personalization for edge platforms, compute-in-memory neural accelerators, and AI-assisted EDA. He received the Best Paper Award at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) in 2023 and a Best Paper Award nomination at ICCAD 2024.

Title: Deploying Edge LLMs for Wafer Defect Detection in Chip Manufacturing

Abstract: Wafer defect detection in chip manufacturing is critical to ensuring yield and reducing costly production delays, yet traditional cloud-based methods struggle with latency and data privacy constraints. This talk explores the deployment of edge-optimized large language models (LLMs) to enable localized, low-latency anomaly detection across fabrication processes. We analyze current edge AI frameworks for manufacturing analytics, highlighting their limitations in handling high-dimensional sensor data and dynamic process variations. The integration of lightweight LLMs with edge computing architectures is presented as a solution, leveraging model compression and hardware-aware optimization to balance accuracy and inference speed. Key challenges, such as maintaining model robustness under resource constraints and adapting to evolving process nodes, are systematically addressed. Finally, we propose future directions for edge LLMs, including federated learning for cross-fab collaboration and hybrid architectures that combine physics-based models with AI-driven insights. This work aims to redefine real-time quality control in semiconductor manufacturing, paving the way for resilient and adaptive production systems.

TECHNICAL SESSIONS

TS 01. System-Level Simulation, Modeling, and Co-Verification

10:40-12:00 | May 10, 2025 @ Sleeping Beauty 1/2

Session Chair: **Gang Qu**, University of Maryland

10:40-11:00 | Invited Talk

Zebo Peng

Linköping University

Bio.: Zebo Peng received his PhD in Computer Science from Linköping University in 1987. He has been Professor and Director of the Embedded Systems Laboratory at Linköping University since 1996. He is also Vice-Chairman of the Department of Computer and Information Science. His research interests include the design and testing of embedded systems, electronic design automation, SoC testing, and real-time systems. He has published more than 400 technical papers and five books in these areas. He has received four best paper awards and one best presentation award at major international conferences. He has been a Golden Core Member of the IEEE Computer Society since 2005 and received the IEEE Computer Society Distinguished Contributor Award in 2022. He has served on the program committee of a dozen international conferences and was Program Chair for DATE 2008 and General Co-Chair for ITC-Asia 2021.

Title: Control/Communication Codesign of Distributed Cyber-Physical Systems

Abstract: In modern cyber-physical systems (CPS), multiple control applications typically share a common distributed computing platform, often spanning an edge-cloud continuum. This transition from dedicated, federated architectures to integrated platforms introduces complex timing behaviors, particularly variable and increased communication delays. These delays—arising from resource sharing and long-range 5G communications—can degrade control performance and, if left unmanaged, even destabilize the system. This talk presents a control/communication codesign framework that integrates delay compensation into both controller synthesis and task scheduling. The framework generates high-quality, stable CPS designs on distributed platforms. By explicitly accounting for the timing effects of shared computational and communication resources, this approach ensures robust and predictable control performance, even in highly dynamic environments.

11:00-11:20 | Paper ID: 60

Title: Codepath: A Performance Simulation Methodology for Multicore Network Processors

Author(s): Shipeng Yue, Honghao Liang, Yu Yang

Presenter: **Shipeng Yue**, Tsinghua University

Abstract: As the number of transistors on a processor chip grows, it takes a longer time to execute the simulation and iterate the architecture design. The performance of current processors is increasingly dependent on software and hardware cooperation. The network processor is a domain-specific processor widely used in routers and switches. Unlike general-purpose processors, network processors need to perform a lot of table lookup operations and execute microcode programs based on the table lookup results, which has a significant impact on chip performance. To speed up the simulation for network processors, we present a performance simulation methodology called codepath. It takes into account the characteristics of realistic network software and simulates the various behaviors of the packets reasonably at a certain abstract level. Compared to RTL (Register Transfer Level) simulation, it can speed up simulations by one or two orders of

magnitude and the average simulation error of packet bandwidth is only 7.36%. The manpower investment can be reduced by 85% for the first version development.

11:20-11:40 | Paper ID: 122

Title: EFSim: An Efficient and Flexible Simulation Framework for Digital In-Memory Computing

Author(s): Qi Cao, Shang Wang, Haisheng Fu, Zhenjiao Chen, Hang Chen, Feng Liang

Presenter: **Qi Cao**, Xi'an Jiaotong University

Abstract: Digital in-memory computing (IMC) has drawn significant attention in neural network acceleration due to its superior energy efficiency and resistance to non-ideal variations. Simultaneously, the rapid evolution of neural networks and the large design space of IMC systems necessitate an early-stage verification simulator. In this paper, we introduce EFSim, an efficient and flexible simulation framework for digital in-memory computing systems. On the hardware level, a parameterized Chisel-based hardware library is constructed to enable the rapid and flexible generation of customized Verilog IMC circuits. On the software level, the IMC inference engine facilitates the efficient deployment of neural network models. Furthermore, EFSim performs hybrid compilation of designed IMC systems using Verilator, thereby enabling rapid performance evaluation and software–hardware co-optimization. Validation through two designed IMC macros demonstrates that the relative modeling error rate of EFSim is below 10%. Experimental results indicate that EFSim enables efficient evaluation of digital IMC systems and supports extensive design space exploration. The EFSim is open-sourced at https://github.com/cq-work/EFSim.

11:40-12:00 | Paper ID: 154

Title: Design of a RISC-V Based Hybrid Encryption Coprocessor for Resource-Constrained Environments

Author(s): Wentao Han, Han Wang, Zhipeng Wu, Yu Liu

Presenter: **Yu Liu**, Tianjin University

Abstract: With the rapid advancement of electronic information technology, data security has become increasingly critical. While hybrid encryption provides higher security compared to traditional single encryption methods, its computational complexity leads to significantly higher resource consumption, making it challenging to deploy in resource-constrained environments. To address this challenge, we propose a RISC-V based hybrid encryption coprocessor designed for the SM2 and SM4 algorithms, achieving an efficient balance between resource utilization and performance. Through custom instruction set design and hardware/software co-optimization, the proposed coprocessor improves both resource efficiency and computational performance while enabling hybrid cryptographic operations. To validate the correctness and efficiency of the design, the coprocessor was integrated with the RISC-V processor and implemented on the Xilinx ZYNQ7020 FPGA. Experimental results show that, the proposed SM2 point multiplication operation achieves an 86.1% reduction in cycle count and a 28.5% decrease in resource consumption, while the SM4 implementation reduces hardware resource usage by 69.3%. These improvements highlight the effectiveness of the proposed design in enhancing the feasibility of hybrid encryption in resource-constrained environments.

TECHNICAL SESSIONS

TS 02. Innovative Simulation and Data Compression for Verification

10:40-12:00 | May 10, 2025 @ Snow White 2/3

Session Chair: Hongce Zhang, The Hong Kong University of Science and Technology (Guangzhou)

10:40-11:00 | Invited Talk

Sybille Hellebrand

Paderborn University

Bio.: Sybille Hellebrand received her Diploma degree in Mathematics from the University of Regensburg, Germany, in 1986. In the same year she joined the Institute of Computer Design and Fault Tolerance at the University of Karlsruhe, Germany, where she received the Ph. D. degree in 1991. Then she was as a postdoctoral fellow at the TIMA/IMAG-Computer Architecture Group, Grenoble, France. From 1992 to 1997 she continued as an assistant professor at the University of Siegen, Germany. Before completing her Habilitation and changing to the Division of Computer Architecture at the University of Stuttgart, Germany, in 1997, she spent several months as a guest researcher with Mentor Graphics Corporation in Portland, Oregon, USA. In 1999 she moved to the University of Innsbruck in Austria as a full professor for Computer Science. Since December 2004, Sybille Hellebrand holds a chair in Computer Engineering at Paderborn University, Germany. In 2014 she was appointed guest professor at Hefei University of Technology in China. Her main research interests include test and diagnosis of micro-electronic systems, in particular built-in test, built-in diagnosis and built-in repair for systems-on-a-chip and networks-on-a-chip, as well as design and synthesis of testable and reliable circuits and systems. She has published numerous papers in international conferences, workshops, and journals. Besides her activities in several program committees, she serves as an associate editor of the Journal of Electronic Testing - Theory and Applications (JETTA).

Title: Low Cost Protection of Streaming Data with Approximate Block Sums

Abstract: In streaming applications the robustness against small deviations can be exploited to minimize crosstalk effects. In this contribution it is shown how approximation for crosstalk avoidance can be efficiently integrated with error detection.

11:00-11:20 | Paper ID: 5

Title: ITE-PBA: A Framework for SMT Solving with If-Then-Else Terms Control Flow and Parallel Branching Assignment in Formal Verification

Author(s): Wenda Leng, Meihua Liu, Yufeng Jin

Presenter: **Wenda Leng**, Peking University

Abstract: Formal verification has become increasingly challenging as integrated circuits continue to grow in complexity. This approach translates hardware description languages into Satisfiability Modulo Theories (SMT) formulas and employs existing SMT solvers for verification. However, current hardware formal verification methodologies typically treat these solvers only as back-end components, which often fails to capture underlying information, thus limiting their performances. To address the concern, this paper introduces ITE-PBA, a novel framework that enhances SMT solving by leveraging If-Then-Else terms originating from data selectors and exploiting their embedded control flow information. In addition, a parallel branching assignment strategy simultaneously applies multiple mainstream and classical assignment schemes, improving the likelihood of identifying effective solutions. Experimental results reveal that integrating ITE-PBA into the Yices2 solver yields speedups of 9.46×.

11:20-11:40 | Paper ID: 182

Title: A Lossless Compression Method for VCD Files Based on Signal Function Relationships, Value Prediction and Bit-Plane Reorganization

Author(s): Zhiqiang He, Gang Chen

Presenter: **Zhiqiang He**, Nanjing University of Aeronautics and Astronautics

Abstract: This paper proposes a VCD file compression method based on signal function relationships, signal value prediction, and bit-plane reorganization. The method aims to address the bottleneck issues related to the storage and transmission of VCD files as the scale of integrated circuit designs continues to grow. The paper develops separate compression strategies for different sections of the VCD file, such as the header, node information, and value change sections, in order to enhance compression efficiency. By analyzing the functional relationships between signals in the value change section and integrating techniques including variable-length encoding, signal value prediction, and bit-plane reorganization, the proposed method significantly improves the compression ratio. The experimental results demonstrate that, for KB-level VCD files, the compression ratio of the method proposed in this paper reaches twice that of other methods. For MB-level files, the compression ratio can reach up to 86.9 times, representing a 142% improvement over existing compression algorithms. Additionally, this paper also addresses special cases, such as the handling of keywords like "$dumpon", ensuring comprehensive optimization and correctness of the compressed VCD files.

11:40-12:00 | Paper ID: 241

Title: ThorSim: Throughput-Oriented Timing Simulation of FinFET Digital Circuits

Author(s): Jan Dennis Reimer, Stefan Holst, Somayeh Sadeghi-Kohan, Hans-Joachim Wunderlich, Sybille Hellebrand

Presenter: **Jan Dennis Reimer**, Paderborn University

Abstract: Accurate timing analysis is crucial for design and verification. In addition, high throughput and scalability are mandatory for simulation-based approaches, which must often cope with high input data volumes and a high number of large circuit instances. Existing approaches using a binary switch model offer an excellent trade-off between accurate SPICE and high-performance gate level simulation in planar CMOS. However, recent experiments have shown that the binary switch model is not accurate enough for FinFET technology. The new approach presented in this paper integrates an enhanced switch-level model into an efficient GPU-based simulation flow. A high throughput is achieved by avoiding event-driven control at the top level, enabling the thread-parallel processing of independent components and input patterns. Experimental results confirm that the new approach accrately predicts the timing of digital circuits in modern CMOS technologies and scales well to multi-million transistor designs.

TECHNICAL SESSIONS

TS 03. Emerging Transistor Technologies and Novel Process Innovations

10:40-12:00 | May 10, 2025 @ Sleeping Beauty 5

Session Chair: **Thai Nguyan**, Intel Corporation

10:40-11:00 | Paper ID: 119

Title: A Multi-Task Neural Network Model for Simultaneous Classification of Light Intensity and Wavelength in 2D Photodetectors

Author(s): Zhixin Chen, Jun Jiang, Zhiyuan Wang, Zichao Ma

Presenter: **Zhixin Chen**, South China University of Technology

Abstract: Accurate extraction of light intensity and wavelength from photodetector responses is essential for decoding information, yet the intertwined influence of the two parameters on device performance poses significant challenges. This study presents a neural network-based model that extracts light intensity and wavelength directly from the current-voltage (I-V) characteristics of 2D materials-based photodetectors. Using a shared-bottom multi-task learning framework, a one-dimensional convolutional neural network (1D-CNN) was employed to capture feature representations from the I-V data, enabling precise classification and extraction of incident light parameters. The model was trained and evaluated using a dataset comprising 3750 I-V curves measured from a high-dynamic range and broadband WSe2/MoS2 heterojunction photodetector. The model exhibits an overall classification accuracy of 99.7%, highlighting the deep learning approach as a data-driven alternative to conventional analytical methods for modeling 2D photodetectors.

11:00-11:20 | Paper ID: 135

Title: A Spatiotemporal Attention Enhanced ConvLSTM Model for Thin Film Deposition Prediction in Semiconductor Manufacturing

Author(s): Kun Pang, Li Ding, Junjie Li, Zhiqiang Li, Hua Shao, Rui Chen, Zhenjie Yao

Presenter: **Zhenjie Yao**, Institute of Microelectronics, Chinese Academy of Sciences

Abstract: In semiconductor manufacturing, the deposition quality of thin film plays a critical role in both production efficiency and device performance. Plasma-enhanced Chemical Vapor Deposition (PECVD) has emerged as a widely adopted technique due to its low process temperature and high deposition rate. A comprehensive understanding of the thin film deposition mechanism of PECVD is essential for optimizing process parameters. This study introduces a Spatiotemporal Attention-enhanced ConvLSTM (STAE-ConvLSTM) model for predicting thin film deposition, specifically modeling the SiOxNy deposition process in PECVD. By integrating advanced spatiotemporal prediction and self-attention techniques, the model effectively captures global spatiotemporal dependencies and the influence of process parameters on film growth. Through extensive testing on diverse datasets, the proposed model demonstrates superior performance in predicting thin film deposition compared to both standard ConvLSTM networks and traditional physical-chemistry-based models. The experimental results highlight the STAE-ConvLSTM model's ability to handle complex substrate structures with high precision. Additionally, long-sequence prediction experiments confirm the model's robustness. The proposed model can predict thin film deposition process effectively.

11:20-11:40 | Paper ID: 137

Title: HC-PINN: A Hard-Constraint Enhanced PINN for Accurate Device-Level Thermal Simulation

Author(s): Honglin Wu, Sihao Chen, Yu Li, Runsheng Wang, Lining Zhang

Presenter: **Honglin Wu**, Peking University

Abstract: In this work, a hard-constraint (HC) enhanced Physics-Informed Neural Network (PINN) framework for accurate device-level thermal simulations is developed, effectively addressing challenges such as complex boundary conditions, multi-material systems, and interface continuity constraints. The approach integrates the domain decomposition method and the mixed residual method (MIM) while enforcing boundary and interface conditions through a hard-constraint strategy, ensuring an improved simulation accuracy. The proposed enhanced PINN thermal simulation framework is verified through its application to advanced silicon-on-insulator (SOI) MOSFETs. Compared with conventional PINN and extended physics-informed neural networks (XPINN) methods, the approach achieves a 4.76× improvement in the MAPE of temperature predictions and significantly enhances the heat flux continuity at material interfaces, ensuring better adherence to physical laws. This work provides a scalable and high-fidelity solution for complex device-level thermal simulations and future semiconductor thermal evaluation and optimization.

11:40-12:00 | Paper ID: 151

Title: Automatic HEMT Device Model Extraction from Document Using AI Agents

Author(s): Yuyang Peng, Zenghui Chang, Yipin Xu, Longchang Wu, Hong Cai Chen

Presenter: **Hong Cai Chen**, Southeast University

Abstract: This study proposes an automated extraction method for HEMT device modeling from technical documents using AI - agent - based models. A data stream - based automation method is proposed, enabling direct HEMT model generation from datasheets. The system includes document parsing, graphical data extraction, parameter extraction using a Chain - of - Thought (CoT) prompting strategy, and SPICE modeling. The ASM - HEMT model, a physics - based compact model, accurately describes GaN HEMTs' properties. The proposed data stream employs EDocDLA for document parsing, EDocCurve for curve extraction, and integrates LLMs and optimization techniques for parameter extraction and model optimization. Experiments on the FHX76LP datasheet demonstrate the data stream's effectiveness. The generated SPICE model has a fitting error below 3% compared to the original data. This automated method significantly enhances modeling efficiency and accuracy, providing an efficient pathway for transforming technical documents into precise device models.

TECHNICAL SESSIONS

TS 04. Emerging Technologies and Applications in EDA

10:40-12:00 | May 10, 2025 @ Snow White 1

Session Chair: Hailong You, Xidian University

10:40-11:00 | Invited Talk

Heng Wu

Peking University

Bio.: Heng Wu is an Associate Professor in the School of Integrated Circuits at Peking University. He received the Ph.D. degree in Electrical and Computer Engineering from Purdue University in early 2016. After graduation, he joined IBM T. J. Watson Research Center in Albany N.Y. USA as a research staff member. He joined Peking University in early 2023.

His research focuses mainly on high speed and low power CMOS devices and circuits, transistors architecture and design technology co-optimization(DTCO). Prof. Wu has published more than 80 papers and received 4 best paper awards (including VLSI symposium). He has filed more than 450 patents (with 150 patents granted). He is an IBM Master Inventor and recipient of IEEE Paul Rappaport Award.

Title: 3D Integration Innovations and Opportunities on Both Sides of Wafer: A Design Perspective

Abstract: As conventional scaling comes to an end, 3D integration emerges as a compelling path forward, offering new dimensions in design flexibility, power efficiency, and density. For here, we present Flip FET (FFET), a new transistor architecture that leverages back-to-back stacking of transistors and interconnects on both sides of wafers, and introduce Flip 3D (F3D) integration, a novel 3D platform featuring dual-side integration. It enables symmetric, dual-sided standard cell design with aggressive cell height scaling down to 2.5 tracks, while maintaining excellent routability and performance.

Multiple innovations to address the complex vertical integration challenges will be addressed, with design techniques like multi-row placement, split gate, and dummy gate insertion also included. Furthermore, the novel dual-sided signal pins and routing capability unlock significant PPA benefits at the block level. Benefited from the dual-sided routing, further frequency gains and metal layer reductions can be achieved.

FFET and F3D not only represent a breakthrough in 3D device-circuit co-design but also provide a practical and manufacturing-friendly path to extend Moore's Law from a design-centric perspective.

11:00-11:20 | Paper ID: 157

Title: Reliable Droplet Routing in Digital Microfluidic Biochips by Reinforcement Learning

Author(s): Qinan Chen, Biao Liu, Chen Jiang, Handing Wang, Tsung-Yi Ho, Bo Yuan

Presenter: **Qinan Chen**, Southern University of Science and Technology

Abstract: In the past decade, digital microfluidic biochips (DMFBs) have emerged as a transformative technology for laboratory automation, yet their clinical adoption remains constrained by reliability challenges stemming from electrode degradation and droplet cross-contamination. In this paper, we propose a contamination-aware cooperative multi-agent reinforcement learning (CaCMARL) framework that addresses the dual challenge of real-time droplet manipulation and cross-contamination minimization. We design a problem-specific observation space and reward function for agents to accomplish the droplet routing task, while minimizing both cross-contamination and completion steps. We accelerate agent training through the introduction of a curriculum learning mechanism. Extensive simulations demonstrate that our proposed

method achieves 47%-58% reduction in cross-contamination events compared to the state-of-the-art method while maintaining similar task success rates and completion steps.

11:20-11:40 | Paper ID: 195

Title: Machine Learning-Assisted Design Automation of Integrated Photonic Devices

Author(s): Yiyang Su, Hao Chen, Yipeng Zang, Qinfen Hao, Yuzhe Ma, Yeyu Tong

Presenter: **Yiyang Su**, Microelectronics Thrust, The Hong Kong University of Science and Technology (Guangzhou)

Abstract: Photonic inverse design has emerged as a transformative approach in the development of integrated photonic devices. The inverse design process primarily relies on two key steps: electromagnetic simulation and optimization algorithms. However, traditional numerical methods for EM simulation often face challenges such as computational inefficiencies, limited data utilization, and a lack of universality. Similarly, conventional iterative optimization algorithms used in inverse design suffer from high computational costs, susceptibility to local optima, and sensitivity to initial conditions. With the rapid advancements in artificial intelligence, machine learning offers a promising avenue to overcome these challenges, enabling efficient automated physical design of high-performance integrated photonic devices without the need for extensive photonics expertise. In this paper, we review several advanced methods that integrate ML into EM simulation and inverse design algorithms. Additionally, we emphasize the importance of incorporating manufacturing constraints to ensure the practical feasibility of the designed devices. By highlighting the potential of ML to revolutionize the design automation of integrated photonic devices, we aim to inspire further research and innovation in this field.

11:40-12:00 | Paper ID: 162

Title: An Efficient Ferroelectric Reconfigurable FET Compact Model for Reprogrammable Circuit Design

Author(s): Weiyi Sun, Bo Li, Guoyong Shi, Wei Mao, Siying Zheng, Jiuren Zhou, Bing Chen, Yan Liu, Genquan Han

Presenter: **Weiyi Sun**, Hangzhou Institute of Technology, Xidian University

Abstract: Reconfigurable field-effect transistor (RFET) is a promising solution to break through the bottleneck of function density and energy efficiency for Post-Moore integrated circuits. This paper develops a Verilog-A implementable compact model for a ferroelectric-based reconfigurable field-effect transistor (Fe-RFET). The model captures the dynamic polarity switching of the Fe-RFET. In addition, novel logic cell circuits based on Fe-RFETs are proposed to achieve the multi-logic function with fewer transistors compared to conventional transistors based and double-gate transistors based cells, showing broad prospect of the application of our developed model.

TECHNICAL SESSIONS

TS 05. Large Language Models and Next-Generation EDA Tools

10:40-11:50 | May 10, 2025 @ Sleeping Beauty 3

Session Chair: **Hao Yan**, Southeast University

10:40-11:10 | Special Invited Talk

Han Yu

Empyrean Technology Co., Ltd

Bio.: Mr. Yu Han received Master Degree of Electronics Engineering from Beihang University and has more than 20 years` experience on full-custom IC design and EDA tools development. He served for Huada Empyrean from 2010, worked as R&D engineer, sr. Application engineer and now sr. technology marketing director. He joined several domestic EDA tools` development and promotion including Empyrean`s Analog/Mixed-signal platform, RF platform, SPICE simulator and dynamic timing & power analysis solution. He is also the main proposer of several domestic standards in EDA field including "Automotive pan-analog integrated circuit EDA technical requirements" etc. In recent years his interest focuses in the development and promotion of AI methods in domestic EDA solutions such as modelling, classifying and calculation.

Title: New Development of AI Used in Full-Custom EDA Solutions

Abstract: This presentation will discuss some potential EDA fields in which AI can help improving efficiency and accuracy such as modeling, classifying, prediction etc. Then it will introduce latest progress of Empyrean's one stop agile full-custom IC design platform using AI assisting circuits generation and migration.

11:10-11:30 | Paper ID: 205

Title: Image2Net: Datasets, Benchmark and Hybrid Framework to Convert Analog Circuit Diagrams into Netlists

Author(s): Haohang Xu, Chengjie Liu, Qihang Wang, Wenhao Huang, Yongjian Xu, Weiyu Chen, Anlan Peng, Zhijun Li, Bo Li, Lei Qi, Jun Yang, Yuan Du, Li Du

Presenter: **Haohang Xu**, Nanjing University

Abstract: Large Language Model (LLM) exhibits great potential in designing of analog integrated circuits (IC) because of its excellence in abstraction and generalization for knowledge. However, further development of LLM-based analog ICs heavily relies on textual description of analog ICs, while existing analog ICs are mostly illustrated in image-based circuit diagrams rather than text-based netlists. Converting circuit diagrams to netlists help LLMs to enrich the knowledge of analog IC. Nevertheless, previously proposed conversion frameworks face challenges in further application because of limited support of image styles and circuit elements. Up to now, it still remains a challenging task to effectively convert complex circuit diagrams into netlists. To this end, this paper constructs and opensources a new dataset with rich styles of circuit diagrams as well as balanced distribution of simple and complex analog ICs. And a hybrid framework, named Image2Net, is proposed for practical conversion from circuit diagrams to netlists. The netlist edit distance (NED) is also introduced to precisely assess the difference between the converted netlists and ground truth. Based on our benchmark, Image2Net achieves 80.77% successful rate, which is 34.62%-45.19% higher than previous works. Specifically, the proposed work shows 0.116 averaged NED, which is 62.1%-69.6% lower than state-of-the-arts.

11:30-11:50 | Paper ID: 32

Title: Sketch-to-Style: Augmenting AI4EDA Dataset with Automatic Image Generative Framework

Author(s): Xinyue Wu, Xinfei Guo
Presenter: **Xinyue Wu**, Shanghai Jiao Tong University

Abstract: While many EDA tools now incorporate machine learning, and data-driven approaches from AI-assisted EDA (AI4EDA) prediction techniques shift the design process left, researchers require increasingly larger datasets to ensure model generalization. However, the scarcity of open-source IP designs, the insufficiency of open-source AI4EDA datasets, and lengthy tool runtimes contribute to the high time, economic, and effort costs of obtaining sufficient data. To address these challenges, we propose a Sketch-to-Style layout image generation framework, which rapidly produces high-quality yet meaningful layout images from limited data. To demonstrate its effectiveness, we focus on generating Design Rule Violation (DRV) feature maps, serving as an augmentation method for DRV prediction—an AI4EDA innovation. Our experiments show that integrating "fake" data from the proposed framework with real datasets steadily improves the performance of Structure Similarity Index Measure (SSIM), while improving 5.11% of the Area Under the Curve of the Receiver Operating Characteristic (AUC of ROC), 32.27% of accuracy and reducing 19.28% of False Positive Rate (FPR) in imbalanced category predictions at the same time, enhancing the model's ability to learn DRV structural features and localization patterns. The proposed framework show great potential of generating image data for various prediction tasks.

TECHNICAL SESSIONS

TS 06. Analog/Mixed-Signal Synthesis and Layout Optimization

14:00-15:40 | May 10, 2025 @ Snow White 1

Session Chair: Keren Zhu, Fudan University

14:00-14:20 | Paper ID: 52

Title: Multi-Armed Bandits-Based Exploring and Exploiting the High-Dimensional Design Space for Analog Circuit with Adjoint Sensitivity

Author(s): Ruiyu Lyu, Yuan Meng, Zhaori Bi, Keren Zhu, Changhao Yan, Fan Yang, Xuan Zeng

Presenter: **Ruiyu Lyu**, Fudan University

Abstract: The continuous expansion of the scale of analog circuits poses significant challenges to the automation of circuit design. This is mainly reflected in the longer simulation time and insufficient exploration of the design space. Traditional optimization algorithms focus on finding optimal points, often overlooking the simulation cost. In this work, we frame the original problem as a multi-armed bandit problem. By applying a Thompson sampling strategy, we achieve a balance between global exploration and local exploitation. During the local exploitation, we propose a sensitivity-guided method ensuring rapid convergence. Experimental results demonstrate that our approach outperforms state-of-the-art techniques, achieving a 5.27x speedup and better global exploratory capabilities.

14:20-14:40 | Paper ID: 57

Title: LLMACD: An LLM-Based Analog Circuit Designer Driven by Behavior Parameters

Author(s): Shaojie Xu, Haochang Zhi, Jintao Li, Weiwei Shan

Presenter: **Shaojie Xu**, Southeast University

Abstract: Analog circuit design is traditionally dependent on extensive human expertise, making the process time consuming and labor intensive. This paper introduces LLMACD, a knowledge-embedded automation designer for analog circuit design based on large language models (LLMs). We design a refined prompt manager to extract circuit representation, embed circuit knowledge, and model the knowledge-intensive design process within a Chain-of-Thought (CoT) workflow. Leveraging LLMs' in-context learning capabilities and high-quality humanannotated design experience, LLMACD derives transistor behavioral parameters by analyzing performance expressions in a human-like manner without complex iterative loops, thereby accelerating the design process. Experimental results demonstrate that LLMACD outperforms traditional iterative transistor sizing optimization methods, achieving faster design times and enhanced circuit performance, with performance gains of up to 2 times.

14:40-15:00 | Paper ID: 64

Title: Design Space Folding: A “Free-lunch” Add-on for Efficient Design Convergence in Transistor Sizing

Author(s): Zhuohua Liu, Yuxuan Zhang, Weilun Xie, Yuanqi Hu, Wei W. Xing

Presenter: **Zhuohua Liu**, Shenzhen University

Abstract: Automatic transistor sizing in circuit design remains a significant challenge. While Bayesian optimization (BO) has shown promise, its optimization process is hindered by large design spaces for most practical circuits, particularly as technology nodes shrink. Inspired by professional analog circuit design workflows where key factors are identified and prioritized in optimization, we propose Design Space Folding (DSFold) to imitate such a process to assist design convergence. The optimization is initially conducted in a folded design space, allowing design points to escape saddle points and converge quickly toward potential

global optima, with the design space progressively unfolding to consider all variables. We assess DSFold by equipping it with many stateof-the-art (SOTA) transistor sizing optimizers on multiple analog circuit benchmarks and show a 1.05x-5.34x speedup and a 1.10x-2.91x convergence performance improvement compared to their original forms with almost zero extra cost (only ~3% computational overhead), achieving significant improvements while maintaining the "free-lunch" advantage.

15:00-15:20 | Paper ID: 70

Title: PZTA: Accelerating Analog Circuit Sizing With A Transferable Circuit Theory-Inspired Pole-Zero Transient Assertion System

Author(s): Xiaoyu Zhong, Jintao Li, Zhaori Bi, Yun Li, Fan Yang, Xuan Zeng, Keren Zhu

Presenter: **Xiaoyu Zhong**, Fudan University

Abstract: Transient simulation is a major computational bottleneck in analog circuit sizing optimization, especially when the circuit is unstable. Simulation-based methods achieve high accuracy but suffer from inefficiency, while surrogate-based approaches promise speedups but struggle with prediction errors and high computational costs. Challenges like poor transferability and reliability constrain their efficacy in accelerating the circuit sizing process. In this paper, we propose an optimization strategy with a transferable pole-zero-based transient assertion (PZTA) system. Inspired by transient analysis theory, the PZTA system is applicable across different topologies and effectively prunes unnecessary simulations with high accuracy. We design an offline-trained neural network model that incorporates circuit theory-inspired features, accurately asserting inferior circuit transient behavior in a zero-shot manner and adaptable to multiple optimization algorithms. Experimental results demonstrate that PZTA system effectively transfers across topologies and prunes over 83.87% of transient simulations exhibiting unstable behavior or inferior performance, with less than 1% false alarms. Our optimizers PZTA-M and PZTA-G on average reduce runtime by 49.54%.

15:20-15:40 | Paper ID: 83

Title: A Large Language Model-based Multi-Agent Framework for Analog Circuits' Sizing Relationships Extraction

Author(s): Chengjie Liu, Weiyu Chen, Huiyao Xu, Yuan Du, Jun Yang, Li Du

Presenter: **Chengjie Liu**, National Center of Technology Innovation for EDA

Abstract: In the design process of the analog circuit pre-layout phase, device sizing is an important step in determining whether an analog circuit can meet the required performance metrics. Many existing techniques extract the circuit sizing task as a mathematical optimization problem to solve and continuously improve the optimization efficiency from a mathematical perspective. But they ignore the automatic introduction of prior knowledge, fail to achieve effective pruning of the search space, which thereby leads to a considerable compression margin remaining in the search space. To alleviate this problem, we propose a large language model (LLM)-based multi-agent framework for analog circuits' sizing relationships extraction from academic papers. The search space in the sizing process can be effectively pruned based on the sizing relationship extracted by this framework. Eventually, we conducted tests on 3 types of circuits, and the optimization efficiency was improved by 2.32 ~ 26.6 \times. This work demonstrates that the LLM can effectively prune the search space for analog circuit sizing, providing a new solution for the combination of LLMs and conventional analog circuit design automation methods.

TECHNICAL SESSIONS

TS 07. High-Level and Behavioral Synthesis: Trends and Optimization

14:00-15:40 | May 10, 2025 @ King Stefan

Session Chair: Zhufei Chu, Ningbo University

14:00-14:20 | Paper ID: 98

Title: FM-AM: Fused-Metrics Approximate Multiplier Exploration Framework for DNNs

Author(s): Xingyu Xu, Zihan Zou, Chen Zhang, Hui Kou, Shikuang Chen, Hao Cai, Bo Liu

Presenter: **Zihan Zou**, Southeast University

Abstract: Quantization combined with approximate computing has been extensively explored in Deep Neural Networks (DNNs) for edge devices and hardware accelerators, offering significant reductions in memory footprint and computation overhead. However, effectively integrating these techniques presents two key challenges: (1) Conventional error metrics, such as mean squared error, fail to accurately capture the proper tradeoff between network accuracy and hardware efficiency. (2) The design space for mixed-precision DNNs is vast, making exhaustive exploration computationally prohibitive. To address these challenges, we propose the Fused-Metrics Approximate Multiplier Exploration (FM-AM) framework, which introduces two key innovations: (1) A cross-layer optimization approach that jointly configures quantization bit-widths and energy-efficient approximate multipliers, guided by fused-metrics error estimation and hardware constraints. (2) A Bayesian Optimization-based search algorithm that efficiently selects approximate computing units by pruning the multiplier library, significantly reducing search time while meeting accuracy requirements. We evaluate FM-AM on AlexNet, ResNet-18, and ResNet-50 using the CIFAR-100 dataset. Experimental results demonstrate energy reductions of 60.2%, 58.9%, and 50.0%, respectively, with only 1.63%, 1.59%, and 1.34% accuracy degradation when implemented in a 28-nm CMOS industrial technology.

14:20-14:40 | Paper ID: 129

Title: PipelineGen: Towards Automated Generation of Pipeline from ISA Formal Semantic Specification

Author(s): Yan Pi, Tun Li, Hongji Zou, Wanxia Qu, Xu He, Wanwei Liu

Presenter: **Xu He**, Hunan University

Abstract: Currently, there are numerous manual factors in microprocessor pipeline design, which may cause problems such as ambiguity in design understanding, low development efficiency, and proneness to errors. In this paper, we propose a method for automatically generating an in-order and single-issue pipeline from formal semantic descriptions of instruction set architecture of a given microprocessor. Based on a divide-and-conquer strategy, an individual datapath for each instruction is synthesized first, and then the datapaths of all instructions are composed into a single datapath using signals-reuse and various proposed techniques, to generate the final pipeline. We implement the proposed method as an open source tool - PipelineGen, which realizes a complete tool-chain from instruction set formal specification to RTL code, and enriches the ecosystem of the Sail language. We evaluate PipelineGen using three typical microprocessor ISAs. PipelineGen can generate correct pipeline designs in minutes, verifying the core concept of ”synthesis is correct”. The promising experimental results demonstrate that our method effectively alleviates the problems in manual pipeline design.

14:40-15:00 | Paper ID: 136

Title: DOMAC: Differentiable Optimization for High-Speed Multipliers and Multiply-Accumulators

Author(s): Chenhao Xue, Yi Ren, Jinwei Zhou, Kezhi Li, Chen Zhang, Yibo Lin, Lining Zhang, Qiang Xu, Guangyu Sun

Presenter: **Chenhao Xue**, Peking University

Abstract: Multipliers and multiply-accumulators (MACs) are fundamental building blocks for compute-intensive applications such as artificial intelligence. With the diminishing returns of Moore's Law, optimizing multiplier performance now necessitates process-aware architectural innovations rather than relying solely on technology scaling. In this paper, we introduce DOMAC, a novel approach that employs differentiable optimization for designing multipliers and MACs at specific technology nodes. DOMAC establishes an analogy between optimizing multi-staged parallel compressor trees and training deep neural networks. Building on this insight, DOMAC reformulates the discrete optimization challenge into a continuous problem by incorporating differentiable timing and area objectives. This formulation enables us to utilize existing deep learning toolkit for highly efficient implementation of the differentiable solver. Experimental results demonstrate that DOMAC achieves significant enhancements in both performance and area efficiency compared to state-of-the-art baselines and commercial IPs in multiplier and MAC designs.

15:00-15:20 | Paper ID: 143

Title: SAT-Sweeping Based on XOR-Majority Graph

Author(s): Jiaxin Peng, Zhang Hu, Yinshui Xia, Lunyao Wang, Zhufei Chu

Presenter: **Jiaxin Peng**, Ningbo University

Abstract: Combinational equivalence checking is a fundamental aspect of electronic design automation (EDA). However, the intricate interconnections of XOR structures in a circuit pose significant challenges for traditional equivalence checking methods. To address these challenges, this paper proposes an equivalence checking method based on SAT-sweeping for XMG networks.

This approach fully exploits the efficiency and compactness of XOR and MAJ logic gates in XMG networks for representing logic functions. It incorporates XMG-specific rewriting optimizations and enhances the traditional SAT-sweeping strategy by introducing a SAT-guided method for generating high-toggle-rate simulation vectors, enabling more efficient verification of internal node equivalence. These improvements collectively enhance the overall verification efficiency. In our experimental results, the final results achieve 2.81$\times$ and 2.74$\times$ improvement compared to state-of-the-art equivalence checking methods.

15:20-15:40 | Paper ID: 145

Title: Area-oriented Boolean Resubstitution with Efficient Dependency Function Computation

Author(s): Chen Lv, Chengyu Ma, Hongyang Pan, Yinshui Xia, Lunyao Wang, Zhufei Chu

Presenter: **Chen Lv**, Ningbo University

Abstract: Boolean resubstitution is a widely recognized and utilized optimization algorithm for logic networks. In this paper, we present an enhancement to the traditional resubstitution approach by integrating the Semi-Tensor Product (STP). Specifically, our novel method leverages STP to compute all feasible dependency functions for a target node in a single calculation during the resubstitution process. By utilizing these dependency functions, we can derive a more optimal implementation for the target node through decomposition and exact synthesis techniques, ultimately leading to more efficient logic network optimization. Experiments on the IWLS benchmark suite demonstrate that our method outperforms state-of-the-art~(SOTA) methods. Specifically, our approach achieves an 7% improvement in the size optimization. In 6-LUT mapping, it achieves an 4.6% improvement in the size-depth product. Furthermore, applying our method after iterating the SOTA resubstitution algorithm until convergence further enhances optimization by 8.17%.

TECHNICAL SESSIONS

TS 08. Physical Design and 3D/2.5D Integration Techniques

14:00-15:40 | May 10, 2025 @ Sleeping Beauty 3

Session Chair: Thai Nguyan, Intel Corporation

14:00-14:20 | Invited Talk

Chen Wu

Ningbo Institute of Digital Twin, Eastern Institute of Technology

Bio.: Chen Wu, got his PhD from UCLA. He is now an assistant researcher at Ningbo Institute of Digital Twin, Eastern Institute of Technology. His research interests include AI Chips (including architecture, instruction set and compiler) and EDA for Chiplets. He has published 20+ papers, got one best paper reward and 5+ patents.

Title: EDA for Chiplet Planning, Design and Verification

Abstract: Chiplets, as a critical technological pathway in the post-Moore era, enable continuous expansion of functionality and performance through heterogeneous integration of multiple chips. However, it is still challenging for current chiplet design methodologies and tools. Automation Challenges: Existing EDA tools (both domestic and international) suffer from low routability, requiring extensive manual intervention. There is an urgent need for automated design tools for system generation, physical planning, placement, and routing. Multi-Physics Simulation Bottlenecks: Conventional field-solver-based multi-physics simulation tools often require layout truncation, leading to excessively long simulation times and incompatibility with incomplete designs. Rapid analysis algorithms for signal integrity (SI), power integrity (PI), electrothermal coupling, and other multi-physics effects are urgently needed. Design-Verification Disconnect: Current fragmented workflows between design and verification tools result in lengthy iterative cycles (design-verify-redesign), sometimes even failing to converge. A "shift-left" design verification process is imperative to reduce iteration overhead. This talk addresses the above pain points by presenting a comprehensive workflow for chiplet physical design and verification. Physical Planning: We introduce methodologies for physical planning that prioritize thermal management, power delivery, and routing feasibility (considering SI/PI constraints). AI-Driven Multi-Physics Evaluation: We propose a data-driven and AI-accelerated multi-physics evaluation model to rapidly predict and optimize performance metrics across electrical, thermal, and mechanical domains.Convergent Design Flow: By integrating the proposed models, we demonstrate a unified design-verification framework that adopts a "shift-left" approach, enabling early-stage validation and significantly reducing iterative cycles.

14:20-14:40 | Paper ID: 192

Title: Leveraging Steiner Tree Grid Segment in GNN for VLSI Pre-Routing Congestion Prediction

Author(s): Xuan Peng, Yi Zou, Xianfeng Song, Yiqiu Liu, Xinting Chen, Shaokun Liu, Xiaoxu Cheng

Presenter: **Xuan Peng**, South China University of Technology

Abstract: Congestion problem is the most critical issue that the very large scale integration (VLSI) industry has to face during physical design. Modern placement and routing tools often optimize performance based on congestion conditions. An accurate congestion prediction model can effectively enhance the quality of placement and routing to effectively reduce the number of time-consuming and computationally-intensive iterations. In this paper, based on the Steiner Tree graph structure, we design a new graph node, GSegment, and propose a Graph Neural Network-based model, STGSG, for binary classification of the routing overflow congestion. Experimental results on real-world designs demonstrate that, compared to the model without using GSegment, our model has an approximately 23% improvement in the F1 score. The experiments proved the key influence of the routing probability calculation based on GSegment on the classification performance.

Our dataset and code can be obtained at https://github.com/pxgh02/STGSG.

14:40-15:00 | Paper ID: 193

Title: RepPart: An Efficient Partitioning Framework with Replication Technique for MFS

Author(s): Haonan Wu, Shunyang Bi, Jing Tang, Hailang Wang, Hailong You

Presenter: **Haonan Wu**, Xidian University

Abstract: The design of large-scale digital integrated circuits (ICs) increasingly relies on logic verification, with FPGA-based hardware emulation emerging as a critical component. Efficient partitioning of the circuit netlist and its mapping to a multiFPGA system (MFS) for emulation has become a key research focus. Due to limited I/O resources, each FPGA is typically connected directly to only a few other FPGAs. Consequently, signal transmission must pass through intermediate FPGAs, which act as hops in the signal path. This phenomenon increases signal delay and degrades overall system performance. This paper introduces RepPart, an efficient partitioning algorithm for multi-FPGA systems designed to simultaneously address multiple constraints. Building on multiple initial partitioning methods, the process is optimized by integrating the fast candidate partition propagation algorithm and the distant root node selection algorithm. Furthermore, solution quality is enhanced by replicating a limited number of critical nodes during the refinement process. Compared to existing approaches, RepPart achieves higherquality zero-hop solutions in significantly less time.

15:00-15:20 | Paper ID: 203

Title: FLPlace: Macro Placement with Forward-Looking Wire Mask Guidance

Author(s): Caiyu Chen, Yue Wu, Xiaoyan Yang

Presenter: **Caiyu Chen**, Hangzhou Dianzi University

Abstract: The development of Very Large Scale Integration (VLSI) technology has introduced new challenges for Electronic Design Automation (EDA) in chip placement. Macro placement is a crucial subproblem in the placement process, focused on determining the positions of all macros to minimize half-perimeter wire length (HPWL) while avoiding overlaps. Recently, wire-mask-guided macro placement methods have shown the potential to achieve promising results for macro placement. However, these methods are prone to getting stuck in local optima, as they focus solely on selecting the current optimal position for placing a macro. In this paper, we proposed a wire-mask-guided macro placement method called FLPlace. Firstly, we presented a forward-looking wire-mask-guided algorithm that accounts for the impact of the current macro's position on subsequent macros, thus optimizing the overall layout. Secondly, we introduced a heuristic space exploration strategy to enhance optimization efficiency. Experimental results on the ISPD2005 and ariane benchmark demonstrate that FLPlace outperforms the wire-mask-guided method WireMask-BBO, achieving an 11.71% optimization in HPWL and converging to a high-quality solution more rapidly.

15:20-15:40 | Paper ID: 219

Title: OASALT: On the Construction of Obstacle-Avoiding Steiner shAllow-Light Tree

Author(s): Wing Ho LAU, Jinwei Liu, Qin Luo, Evangeline F.Y. Young

Presenter: **Wing Ho LAU**, The Chinese University of Hong Kong

Abstract: In routing tree generation, two important metrics are introduced to evaluate the quality. Wirelength (WL) is directly related to power consumption, routing resource usage and wire delay while pathlength (PL) is indicative of the wire delay. SALT and PD-II are the leading algorithms for the construction of shallow-light routing trees. However, they cannot handle the real designs with blockages. In this paper, we extended the SALT to be Obstacle-Avoiding Steiner shAllow-Light Tree (OASALT) to handle obstacles. First, we improve the time complexity of Lin's Obstacle-Avoiding Spanning Graph (OASG) from $O(n^2 \log n)$ to $O(n^2)$. In addition, we extended the CL algorithm to generate Obstacle-Avoiding Rectilinear Steiner Minimum Arborescence (OARSMA). The experiment shows that OASALT can achieve a better tradeoff between WL and PL under the cases with obstacles, by combining Obstacle-Avoiding Rectilinear Steiner Minimum Tree (OARSMT) and OARSMA. Compared to performance-driven Obstacle-Avoiding Rectilinear Steiner Tree (PDOARST), OASALT improves the worst delay by 15% and WL by 10% on average.

TECHNICAL SESSIONS

TS 09. Reliability Engineering and Post-Layout Optimization

14:00-15:50 | May 10, 2025 @ Snow White 2

Session Chair: Yu-Guang Chen, National Central University

14:00-14:30 | Special Invited Talk

Weiwei Pan

Semitronix Corporation

Bio.: Dr. Weiwei Pan graduated from Zhejiang University with a Ph.D. in Circuits and Systems. With over a decade of experience in the field of Integrated Circuits, she currently serves as the Vice President of Technology at Semitronix Corporation, leading the development of EDA software. Over the years, Dr. Pan has dedicated herself to research related to advanced process design and yield enhancement technologies in integrated circuits. Her expertise encompasses circuit design for yield improvement, design for manufacturability, EDA tools development, and yield enhancement solutions

Title: Shaping the Future of Semiconductor Design with Pattern-Driven Solutions: Innovations, Applications, and Roadmap

Abstract: In today's semiconductor industry, the pressure to innovate at ever-shrinking nodes while maintaining high yields has never been greater. Traditional design methods often struggle to address the increasing complexity of process variations, limiting both performance and manufacturability. This is where Pattern-Driven solutions come in—offering a smarter, more adaptive approach to semiconductor design.

At Semitronix, we've developed a cutting-edge Pattern-Driven solution that seamlessly integrates with existing workflows to optimize design layouts, ensure manufacturability, and significantly reduce time-to-market. By leveraging advanced machine learning and key simulations, our solution anticipates potential manufacturing issues early, providing real-time, actionable insights.

With proven success in high-density applications, our solution not only improves yield but also enhances design-to-manufacturing alignment, resulting in lower costs and better performance. Our roadmap further expands on these capabilities, introducing next-gen optimizations and AI-driven advancements to meet the evolving needs of the semiconductor industry.

Join us as we explore how Pattern-Driven technology is poised to transform the way we design and manufacture the next generation of semiconductors.

14:30-14:50 | Paper ID: 133

Title: New Approach for Aging Assessment of Digital Circuits Featuring Systematic Signal Probability Tracing

Author(s): Yaqi Sun, Feiyang Shu, Muyan Jin, Pengpeng Ren, Runsheng Wang, Zhigang Ji

Presenter: **Yaqi Sun**, Shanghai Jiao Tong University

Abstract: Digital circuit reliability is increasingly challenged by aging effects, particularly Bias Temperature Instability (BTI), which gradually shifts threshold voltages, degrades key electrical parameters, and exacerbates timing violations. To address these challenges, this paper proposes a systematic and efficient methodology for digital circuit aging assessment which is fully compatible with existing design flows. Our approach introduces a two-tiered framework that first derives cell-level signal probabilities (SP) from circuit-level analysis, and then leverages cell-level SPs to evaluate device-level BTI per cell. By utilizing an accelerated algorithm that derives cell-level SP directly from the synthesized netlist, our method eliminates dependence on simulation tools,

thereby reducing the overall run-time and greatly improving the efficiency of aging assessment. Through a graph-based algorithm, device BTI per cell is determined and this process is integrated into the aging library characterization flow. Furthermore, our iterative technique for sequential cells efficiently resolves SP calculation problems of feedback loops, allowing accurate SP calculation throughout the entire design. Experimental results on the ISCAS85 and EPFL benchmarks demonstrate an average runtime speedup of 18.44× while verifying the correctness of the proposed method on simple benchmark circuits. Moreover, the runtime advantage becomes even more pronounced for larger-scale circuits.

14:50-15:10 | Paper ID: 178

Title: Efficient Polynomial Chaos Expansion Method based on Tensor Train Decomposition for High-Dimensional Yield Analysis

Author(s): Hao Zhou, Quan Chen

Presenter: **Hao Zhou**, Southern University of Science and Technology

Abstract: With the advancement of technology, process variations have a critical impact on key IC designs. Accurately and efficiently estimating circuit failure rates under process variations has become increasingly challenging due to the "curse of dimensionality" introduced by a large number of random variables. Traditional Monte Carlo methods incur prohibitively high computational costs. In this paper, we propose a meta-modeling approach that integrates polynomial chaos expansion(PCE) with low-rank tensor approximation to effectively address these challenges. This method mitigates the "curse of dimensionality", ensuring that computational cost scales linearly with dimensionality. Specifically, we employ tensor train (TT) decomposition to achieve a low-rank approximation of the original tensor, demonstrating superior performance in SRAM column circuit simulations. Compared to CANDECOMP/PARAFAC(CP) decomposition, the TT-based approximation offers greater accuracy and stability. Additionally, we incorporate sensitivity analysis to further reduce computational costs.

15:10-15:30 | Paper ID: 200

Title: Enhanced SEM Image Denoising via U-Net Based GAN Using Multi-Die Single Frame Images

Author(s): Yanjiang Li, Zhiping Mou, Shibin Xu, Yongyu Wu, Kun Ren, Dawei Gao

Presenter: **Yanjiang Li**, Zhejiang University

Abstract: With the advancement of integrated circuit technology nodes, distortion occurs in pattern transfer inevitably caused by Optical Proximity Effect (OPE). Model-based OPC (MB-OPC) is the most commonly used solution in the industry. MB-OPC relies on an accurate lithography model to guide it. However, numerous challenges are in face when tuning a lithography model. Scanning Electronic Microscope (SEM) images—the most critical data for lithography model tend to be noisy. The current method of image denoising is frame averaging, but it's time-consuming and affected by resist shrinkage, leading to inaccuracy model. Deep learning methods in previous study lack real and accurate SEM images. We collected reliable SEM images from a fab by overlying Multi die single frame images, and a UNet-based GAN model is designed for denoising. Experiment demonstrates that MSE, PSNR, and SSIM of our methods are at least 9.1%, 2.7% and 1.4% better than other methods. Moreover, our method outperforms other methods in preserving process metrics like line widths and contour accuracy, closely approximating the target images.

15:30-15:50 | Paper ID: 216

Title: Masked Layout Modeling Advances Hotspot Detection

Author(s): Binwu Zhu, Zhengzhou Gu, Jinbin Deng, Yuzhe Ma

Presenter: **Binwu Zhu**, Southeast University

Abstract: With the rapid advancement of semiconductor technology and the continuous miniaturization of circuit feature sizes, hotspot detection has become an increasingly critical yet challenging task in physical

verification workflows. In recent years, numerous deep learning frameworks have been developed to address hotspot detection. However, the performance of these learning-based frameworks is heavily dependent on the quality of the datasets used. However, obtaining a large labeled hotspot dataset with high quality is an extremely time-consuming process. Recently, masked image modeling (MIM) has drawn significant attention for its ability to learn from vast amounts of unlabeled data and has demonstrated effectiveness across a wide range of image tasks. Despite its success, the application of MIM to layout analysis, particularly in the context of semiconductor design, remains largely unexplored. Motivated by the principles of MIM, we propose a transfer learning framework that leverages pretraining through masked layout modeling (MLAM) and subsequently fine-tunes the model on limited labeled hotspot detection datasets. Experimental results on our custom layout datasets demonstrate the effectiveness of our approach.

TECHNICAL SESSIONS

TS 10. AI-Driven Design Automation and Open Source Initiatives

14:00-15:40 | May 10, 2025 @ Sleeping Beauty 1/2

Session Chair: **Changkai Yu**, Jaguar Micro

14:00-14:20 | Paper ID: 112

Title: An Effective Fixed-Outline Floorplanning Algorithm for Rectilinear Soft Modules

Author(s): Yichen Lu, Fuxing Huang, Ziran Zhu

Presenter: **Yichen Lu**, Southeast University

Abstract: The increasing demand for flexible module integration necessitates the placement of rectilinear soft modules, which pose significant challenges in floorplanning, particularly under fixed-outline constraints and with pre-placed modules. In this paper, we propose an effective fixed-outline floorplanning algorithm for rectilinear soft modules. We first present electrostatics-based global floorplanning with a module-area-growing strategy to optimize the positions and dimensions of soft modules. Then, a negotiation-based legalization method is proposed to eliminate overlaps between modules, where a polygonal shape determination method for rectilinear soft modules is presented to minimize wirelength while considering polygonal shape constraints. Finally, a polygon-clipping-based refinement method is developed to further optimize both shape and wirelength. Based on the GSRC and MCNC benchmarks, experimental results demonstrate that our algorithm achieves a smaller half-perimeter wirelength (HPWL) in a reasonable runtime.

14:20-14:40 | Paper ID: 128

Title: AnalogXpert: Automating Analog Topology Synthesis by Incorporating Circuit Design Expertise into Large Language Models

Author(s): Haoyi Zhang, Yibo Lin, Runsheng Wang, Shizhao Sun, Jiang Bian

Presenter: **Haoyi Zhang**, Peking University

Abstract: Analog topology synthesis is one of the major challenges in analog design automation since the topology of analog circuits has a large design space and contains a lot of human expertise. Traditional methods suffer in generating high-quality topology due to the diversity of topologies and the lack of ability to understand human experience. Therefore, LLM has been adopted in recent studies to generate such topologies. However, most of the existing work utilizes ideal modelbased generation or ambiguous design requirements, both of which are not in line with industrial practice and require additional effort. In this work, we propose AnalogXpert, an LLM-based agent formulating topology synthesis as subcircuit-level SPICE code generation which is more practical. AnalogXpert incorporates circuit design expertise by introducing a proofreading strategy that allows LLMs to incrementally correct the errors in the initial design. Finally, we construct a highquality benchmark validated by both real data (30) and synthetic data (2k). AnalogXpert achieves 40% and 23% success rates on the synthetic dataset and real dataset respectively, which is markedly better than those of GPT-4o (3%,3%) and AnalogCoder (8%,6%).

14:40-15:00 | Paper ID: 140

Title: ForgeEDA: A Comprehensive Multimodal Dataset for Advancing EDA

Author(s): Zhengyuan Shi, Zeju Li, Chengyu Ma, Yunhao Zhou, Ziyang Zheng, Jiawei Liu, Hongyang Pan, Lingfeng Zhou, Kezhi Li, Jiaying Zhu, Lingwei Yan, Zhiqiang He, Chenhao Xue, Wentao Jiang, Fan Yang, Guangyu Sun, Xiaoyan Yang, Gang Chen, Chuan Shi, Zhufei Chu, Jun Yang, Qiang Xu

Presenter: **Zhengyuan Shi**, The Chinese University of Hong Kong

Abstract: We introduce ForgeEDA, an open-source comprehensive circuit dataset across various categories. ForgeEDA includes diverse circuit representations such as Register Transfer Level (RTL) code, Post-mapping (PM) netlists, And-Inverter Graphs (AIGs), and placed netlists, enabling comprehensive analysis and development. We demonstrate ForgeEDA's utility by benchmarking state-of-the-art EDA algorithms on critical tasks such as Power, Performance, and Area (PPA) optimization, highlighting its ability to expose performance gaps and drive advancements. Additionally, ForgeEDA's scale and diversity facilitate the training of AI models for EDA tasks, demonstrating its potential to improve model performance and generalization. By addressing limitations in existing datasets, ForgeEDA aims to catalyze breakthroughs in modern IC design and support the next generation of innovations in EDA.

15:00-15:20 | Paper ID: 173

Title: Spec2Doc2RTL: RTL Generation from Specification with Natural Language Representation

Author(s): Zihao Chen, Zihan Lin, Xinhua Chen, Zhiyi Liu, Changxu Liu, Yuxuan Qiao, Yifei Feng, Junjie Zuo, Yifan Song, Fan Yang

Presenter: **Zihao Chen**, Fudan University

Abstract: This paper presents Spec2Doc2RTL, a hierarchical LLM-based RTL code generation framework leveraging natural language as the intermediate design representation. To address the complexity of design hierarchies and circuit diversity, we propose a universal recursive decomposition method that transforms the circuit design process into the nested module implementations. We introduce a register-transfer-level (RTL) code generation pipeline from design specifications based on natural language representation, which includes two LLM-friendly stages: design document generation (Spec2Doc) and document-to-RTL translation (Doc2RTL). Moreover, a fully automated iterative design workflow is implemented, with script generation, testing, and debugging integrated. Experimental results demonstrate that Spec2Doc2RTL can generate a wide spectrum of circuits, from complex systems like CPUs and NTTs to foundational bottom-level modules with a competitive 78.8% accuracy on the Revisiting VerilogEval benchmark.

15:20-15:40 | Paper ID: 174

Title: MF-VIT: Lithography Hotspot Detection Based on Multi-scale Feature and Vision Transformer

Author(s): Zhou Huang, Zhigang Li, Ming Zhu, Bo Wu, Peifei Chen

Presenter: **Zhou Huang**, Anhui University

Abstract: As the size of chips continues to shrink, the optical proximity effect becomes increasingly pronounced. Lithography hotspots, such as open circuits or short circuits, may manifest during the manufacturing process, adversely impacting chip yield and reliability. Although deep learning has been widely applied to hotspot detection, challenges remain in achieving high recall and precision. In this paper, we propose a hotspot classification model MF-VIT based on an improved Vision Transformer, addressing these challenges using a multi-scale feature fusion strategy. In addition, the Focal Loss function is introduced to effectively mitigate the issue of imbalanced lithography hotspot data. Comparative experiments on the ICCAD-2012 Contest benchmarks demonstrate that the proposed method achieves superior classification performance, yielding an overall average recall rate of 98.5%.

TECHNICAL SESSIONS

TS 11. Innovations in Memory Architecture and Near/In-Memory Computing

16:00-18:00 | May 10, 2025 @ Snow White 3

Session Chair: Li Du, Nanjing University

16:00-16:20 | Paper ID: 97

Title: A Hybrid Encryption Framework for Federated Learning Accelerated on RRAM

Author(s): Lingyao Li, Xing Mou, Jingxiang Ren, Qisheng Yang, Yaohua Wang

Presenter: **Qisheng Yang**, Hunan University

Abstract: Federated learning (FL) enables decentralized collaborative training while preserving data privacy, yet it remains vulnerable to dual privacy threats: client-side training data inference attacks and server-side insecure aggregation. To address these challenges, this study proposes a hybrid encryption framework accelerated on Resistive Random Access Memory (RRAM) that integrates differential privacy (DP) and homomorphic encryption (HE) for multilevel security protection. The framework innovatively harnesses two key characteristics of RRAM devices: (1) The parallel in-memory computing capability enabled by crossbar array architectures reduces the computational complexity of HE-based matrix encryption, achieving real-time encryption throughput; (2) The stochastic cycle-to-cycle read noise inherent to RRAM devices is systematically harnessed as a DP-compliant noise injection mechanism, enabling tunable privacy budgets without additional computational overhead. Experiments demonstrate that the proposed scheme achieves a privacy budget of 1.737 to 5.791 on the CIFAR-10 dataset while maintaining a negligible accuracy loss (1% to 4%). Benchmark results reveal a 270x acceleration over CPU implementations. This framework provides a new hardware implementation path for privacy-preserving machine learning on resource-constrained edge devices.

16:20-16:40 | Paper ID: 110

Title: BBP-DNS: Batch-Block Parallelism and Dual-NoC Scheduling for Accelerating GPT on Edge Devices

Author(s): Shuai Yuan, Dan Niu, Huatao Zhao, Shiyuan Liu, Zhou Jin, Changyin Sun

Presenter: **Dan Niu**, Southeast University

Abstract: Transformer-based GPT models in artificial intelligence have exhibited remarkable performance advantages across generative tasks. However, edge-side deployment of GPT models faces significant challenges due to the limited memory and computational resources of edge devices. The lack of specialized compiler toolchains often necessitates manual compilation, resulting in complicated deployment processes. To address these challenges, we propose a Batch-Block Parallelization and Dual-NoC Scheduling algorithm(BBP-DNS) for edge devices, which automates tensor partitioning and batch scheduling to enhance data locality and reduce overheads in data storage, movement, and kernel scheduling, thereby improving inference speed. To mitigate hardware constraints in accelerator memory, bandwidth, and compute resources, we extend tensor parallelism with a fine-grained batch-level scheduling strategy. Additionally, we introduce a novel operator mapping methodology that automates accelerator data management, addressing the inefficiencies of traditional manual compilation workflow. Experimental results demonstrate BBP-DNS's superior performance, achieving a 30x performance improvement of a GPT single-layer block on simulator of that evaluated by TVM and PyTorch on CPUs.

16:40-17:00 | Paper ID: 156

Title: An Efficient Single-Cell Associative Search Engine via Conditional Execution

Author(s): Jiayi Wang, Yu Qian, Zeyu Yang, Zheyu Yan, Cheng Zhuo, Xunzhao Yin

Presenter: **Jiayi Wang**, Zhejiang University

Abstract: Content addressable memories (CAMs) embed parallel associative search directly into memory blocks, making them essential for associative memory (AM) applications. CAMs can efficiently perform best or exact search operations that identify a data entry in the database that is the closest or exactly the same as the input entry, respectively. Recently, a single FeFET-based design that is compact and highly efficient has been proposed. However, its multi-step sensing scheme is tailored for best search and is thus inefficient for exact search operations. To address this, we propose a sensing scheme with the concept of conditional execution that dynamically prunes execution steps according to the outputs of the early steps. For higher efficiency, we implement the proposed sensing scheme in the voltage domain and propose an efficient transformation scheme to support current domain arrays. The proposed scheme achieves up to 3.66x and 3x lower energy and latency respectively. The proposed method also achieves a 2.5x lower error rate.

17:00-17:20 | Paper ID: 224

Title: NandPIM: An Optimization Framework for 2D/3D NAND-Based PIM Featuring Genetic Algorithm-based Search of Design Space

Author(s): Fanzi Meng, Xiapeng Xu, Tianze Wu, Xiaojiang Guo, Xinxin Xu, Qiang Tang, Liang Zhao

Presenter: **Liang Zhao**, Zhejiang University

Abstract: This paper presents NandPIM, an innovative NAND flash-based processing-in-memory (PIM) accelerator design coupled with an automatic deep neural network (DNN) quantization framework. By integrating spatial partition mapping and weight duplication strategies, NandPIM fully leverages the high-density storage capability of NAND flash memory and significantly improves computational parallelism. Moreover, alternating mapping of weights within the flash memory array improves the effective endurance of the PIM system. The quantization framework of NandPIM, powered by a Genetic Algorithm, automatically optimizes the bit-widths of DNN weights to determine the optimal layer-by-layer quantization strategy within the constraints of hardware resources and inference accuracy. Experimental results demonstrate that the proposed design outperforms traditional PIM approaches in terms of area, latency and energy efficiency. Furthermore, NandPIM achieves automatic bit-width compression across various DNN models, boosting the computational efficiency while preserving the model accuracy. This framework provides a compelling solution for the efficient deployment of DNNs on 2D/3D NAND-based PIM chips.

17:20-17:40 | Paper ID: 238

Title: Enabling High-Throughput Inference of Transformers on Near-Data Processing Architectures

Author(s): Yingjian Zhong, Qin Xu, Mengke Ge, Song Chen

Presenter: **Yingjian Zhong**, Anhui University

Abstract: The rapid adoption of Transformer models in AI has exposed critical inefficiencies in conventional computing architectures, particularly due to their large memory footprint and low data reuse. Near-Data Processing (NDP) architectures have emerged as a promising solution to mitigate the memory wall problem, especially for memory-intensive neural network(NN) workloads. However, existing AI compilation frameworks, optimized for von Neumann architectures, fail to exploit the distributed nature and fine-grained parallelism inherent in the NDP architectures, especially for memory-intensive Transformer models. This work proposes a mapping framework that leverages novel pipeline parallelism to maximize the inference throughput of Transformers on NDP architectures. Firstly, we propose a pipeline layout strategy called Rect-zigzag, which offers superior flexibility compared to existing pipeline layout strategies (such as 1D static layout and zigzag layout) while adapting to the fine-grained partitioning required by Transformer models. Secondly, we propose a dynamic programming-based mapping algorithm capable of achieving joint optimization of partitioning and pipeline layout for Transformer models. Experiments demonstrate that our mapping method enables the inference throughput of Transformers to reach 1.14 ~ 3.92× that of the baseline methods.

17:40-18:00 | Paper ID: 239

Title: Fe-NVSim: An Extended NVSim for Emerging FeFET-based Embeded Memory Simulation

Author(s): Kai Chen, Junfeng Tan, Bo Li, Xiguang Wu, Kai Xiong, Hongrui Zhang, Bing Chen, Yan Liu, Genquan Han

Presenter: **Bo Li**, Xidian University

Abstract: Ferroelectric field effect transistors (FeFETs) exhibit significant potential in emerging non-volatile memory (NVM) applications. There is an increasing need to evaluate and explore the design space of FeFET-based memory. However, FeFET are not well supported in current simulation tools such as NVSim and DRAMsim3 due to the unique properties of FeFET. In this paper, we present a comprehensive implementation methods to estimate the area, energy consumption and latency of multiple FeFET memory cell to extend the functionality of the circuit-aware simulator NVSim. In addition, it enables the unique performance estimation of multi-level FeFET memory arrays and the memory window under different ferroelectric materials and ferroelectric layer structures. The effectiveness and reliability of Fe-NVSim have been simulated and discussed. Fe-NVSim is anticipated to facilitate FeFET memory circuit design.

TECHNICAL SESSIONS

TS 12. Advanced Floorplanning and Macro Placement

16:00-17:40 | May 10, 2025 @ Sleeping Beauty 1/2

Session Chair: **Hailong Yao**, University of Science and Technology Beijing

16:00-16:20 | Paper ID: 31

Title: IncreDFlip: Incremental Dataflow-Driven Macro Flipping for Efficient Macro Placement Refinement

Author(s): Xiaotian Zhao, Jiayin Chen, Zixuan Li, Yichen Cai, Xinfei Guo

Presenter: **Xiaotian Zhao**, Shanghai Jiao Tong University

Abstract: Macro flipping is a simple yet effective action for improving wirelength and timing during chip floorplanning. However, in modern macro or mixed-size placers, flipping is often just one tool among many in a broad toolkit aimed at optimizing wirelength within certain thresholds. This approach has created an expansive search space due to the growing number of macros, leading to less-than-ideal macro placement outcomes because the significance of macro flipping is frequently underestimated. In this paper, we highlight the importance of incremental macro flipping and introduce IncreDFlip, a methodology that leverages dataflow information to narrow the search space and utilizes dataflow decomposition from the synthesized netlist to guide flipping decisions. Drawing inspiration from human floorplanning strategies, we further propose fine-tuning techniques to enhance dataflow-driven flipping actions. The combined approach achieves an average improvement of 4.87% in total routed wirelength compared to non-flipped macro placement results, outperforming flipping actions in state-of-the-art macro and mixed-size placers, including DREAMPlace 4.1, AutoDMP, and a commercial tool by 5.03%, 4.48%, and 2.06%, respectively. Additionally, it offers a 4.30% improvement in routed wirelength over the flipping-aware dataflowdriven placer, Hier-RTLMP. Furthermore, our method delivers an average improvement of 14.00% in worst negative slack (WNS) and 32.48% in total negative slack (TNS) after routing, along with a 43.59% reduction in runtime compared to Hier-RTLMP.

16:20-16:40 | Paper ID: 34

Title: Multi-Row Standard Cell Layout Synthesis with Enhanced Scalability

Author(s): Kairong Guo

Presenter: **Kairong Guo**, Peking University

Abstract: Multi-row standard cells are widely adopted in advanced technology nodes, especially for complicated and large cells like multi-bit flip-flops(MBFFs). Due to reduced cell heights and routing tracks, designing standard cell layouts in advanced technology nodes becomes increasingly challenging. Automatic standard cell layout synthesis is being actively explored. However, existing methods face scalability issues when synthesizing large-scale multi-row cells. In this paper, we propose a multi-row cell layout synthesis flow that addresses such scalability issue through a hierarchical approach, including transistor clustering, SMT-based row assignment, transistor-level and cluster-level placement, and genetic algorithm based sequential routing, which collectively enables efficient handling of large-scale designs. Experimental results on an industrial 7nm FinFET library demonstrate the ability to handle designs with up to 152 transistors, achieving area reductions up to 23% on large MBFF cells and reducing runtime by up to 36× compared to prior methods.

16:40-17:00 | Paper ID: 36

Title: Point-Cap: An Efficient Model for Chip-scale Interconnect Capacitance Extraction

Author(s): Weizhe Zhang, Yaohui Han, Lihao Liu, Qunsong Ye, Fan Yang, Tinghuan Chen

Presenter: **Weizhe Zhang**, Chinese University of Hong Kong, Shenzhen

Abstract: In this paper, we present a PointNet++-based method for capacitance extraction (Point-Cap) of chip-scale interconnects with high efficiency and accuracy. By modeling the layout structure as point-cloud-like data, the process of gathering features of conductors to the net level can be done efficiently and automatically by our model and then utilized to predict precise total capacitance and coupling capacitance. Compared to the previous state-of-the-art work, GNN-Cap, Point-Cap reduces the average relative errors in the total capacitance and coupling capacitance calculations by 28.8% and 38.6%, respectively.

17:00-17:20 | Paper ID: 69

Title: NOIP: Node Overlay Initial Partitioning Technique for Hypergraph Partitioning Problem

Author(s): Jing Tang, Shunyang Bi, Hailang Wang, Haonan Wu, Qiwang Chen, Kexin Zhang, Hailong You

Presenter: **Jing Tang**, Xidian University

Abstract: The hypergraph partitioning problem with the goal of minimizing the cut-size has extensive applications in the field of EDA. As an NP-hard problem, the industry commonly uses heuristic-based multilevel partitioning schemes to solve this problem. However, some well-known partitioners, like hMETIS and KaHyPar, each stage in the partitioning process is relatively independent, failing to make full use of the existing partitioning information. We propose a novel initial partitioning algorithm named Node Overlay Initial Partitioning (NOIP). This algorithm uses the existing partitioning results in the initial partitioning to find the fixed vertices at the maximum degree of overlay, and these fixed vertices are used to guide the subsequent initial partitioning. Through experiments based on Titan23, the partitioner integrated with NOIP can achieve a cut-size 0.86 times that of hMETIS within comparable time. Meanwhile, its characteristic of making full use of existing information during the partitioning process also brings new idea to the multilevel partitioning scheme, which enables the partitioner to achieve better results without consuming more time and resources.

17:20-17:40 | Paper ID: 89

Title: DieRouter+: Enhancing Die-Level Routing with SOCP and Scheduler-Driven DP

Author(s): Qifu Hu, Ruyang Li

Presenter: **Qifu Hu**, Shandong Massive Information Technology Research Institute

Abstract: Verifying functional correctness is a key challenge in VLSI design. FPGA prototyping balances runtime and cost in logic verification and is widely used for large-scale circuit verification. To accommodate the increasing complexity of circuits, it extends from a single FPGA to a Multi-FPGA System (MFS), a network of interconnected FPGA dies. Die-level routing, which determines a routing topology and its corresponding Time-Division Multiplexing (TDM) assignment scheme, is crucial for maximizing the operating frequency of MFS. This paper presents DieRouter+, an improved die-level router built upon DieRouter, the first published solution to this problem. DieRouter+ introduces three key innovations: (1) a simpler yet more effective initial routing method based on shortest path trees, (2) a Second-Order Cone Programming formulation of an extended relaxed TDM assignment problem to compute optimal continuous TDM ratios, thereby improving the optimality of the legalized TDM assignment derived from these ratios, and (3) a scheduler-driven Dynamic Programming (DP) based legalization technique that adaptively schedules state evaluations, reducing the number of state evaluations by about 50% compared to the original DP in DieRouter. We evaluate DieRouter+ on 10 benchmark test cases from the 2023 EDA Elite Design Challenge. It outperforms both the competition's 1st-place method and DieRouter, reducing the maximum net delay by 10.12% and 5.71% on average for 5 challenging cases with up to millions of nets, while maintaining comparable performance on easier cases with at most a few thousand nets. Additionally, for large-scale instances, DieRouter+ achieves a 40% speedup over DieRouter. These results confirm the effectiveness of DieRouter+ in optimizing die-level routing.

TECHNICAL SESSIONS

TS 13. Design-Technology Co-Optimization and Manufacturability

16:00-18:00 | May 10, 2025 @ King Stefan

Session Chair: **Keren Zhu**, Fudan University

16:00-16:20 | Invited Talk

Wenchao Liu

Primarius Technologies CO.,LTD.

Bio.: Dr. Liu Wenchao, currently serving as Vice President at Primarius and General Manager of Primarius Technologies Guangzhou Branch. He has more than 20 years of experience in technology research and management at international semiconductor companies, also his work areas cover chip manufacturing, IC design, and electronic design automation (EDA). In 2004, he obtained a doctor's degree in microelectronics and solid state electronics from Shanghai Institute of Microsystem and Information Technology; From 2004 to 2005, he served as the Principal Engineer of HHGrace; From 2005 to 2009, he served as the Principal Engineer of IBM Semiconductor R&D Center in the United States; From 2009 to 2018, he also served as Senior Technical Manager in Singapore Chartered Semiconductor and GLOBALFOUNDRIES; From 2018 to 2019, served as the Design Platform Director of Unisoc Technologies.

Title: Application Driven One-stop Reliability Solution

Abstract: Semiconductor technology advancement has elevated reliability to a crucial design role, particularly in safety-critical industries such as automotive and aerospace. Operating environments characterized by extreme temperatures, radiation exposure, and sustained stress require integrated circuits engineered to resist long-term performance degradation. Meeting these challenges requires comprehensive reliability solutions that integrate predictive modeling with design verification methodologies. This presentation explores how reliability-aware methodologies, combined with advanced measurement instrument FS800™ and EDA tools like BSIMProPlus™ (for aging-aware modeling platform) and NanoSpice™ (for high-accuracy reliability analysis), enable a streamlined workflow—from early-stage failure prediction to sign-off. Companies leveraging these solutions can ensure compliance with strict standards while optimizing performance and yield. This one-stop approach empowers engineers to deliver safer, more durable chips with accelerated time-to-market.

16:20-16:40 | Paper ID: 22

Title: Constrained MRC Approaches for Inverse Lithography

Author(s): Xiaoxuan Liu, Peixian Zheng, Yuhang Wang, Yijiang Shen, Hong Chen

Presenter: **Yijiang Shen**, Guangdong University of Technology

Abstract: The dramatically evolved optical proximity correction (OPC) in lithographic process and mask manufacturing is requiring the notion and practice of curvy features in industry to improve printability and pattern fidelity. However, the pragmatic manufacturability of curvy features requires reliable mask rule checks (MRCs), as a consequence, addressing MRC violations is critical in optical proximity correction (OPC) engines. In this paper, we propose a constrained approach for curvy feature MRC compliance where a skeleton-distance map-based method is implemented for MRC violation detection and correction, and a mask rule penalty term per correction with the mask contour as a distance indicator is incorporated into the level-set based optimization process to avoid local rule-violation level-set evolution. Simulation results demonstrate that the constrained approach penalizes the occurrence of mask rule violations and resolve MRC violations without degrading imaging performance.

16:40-17:00 | Paper ID: 198

Title: DATIS: DRAM Architecture and Technology Integrated Simulation

Author(s): Shiyu Xia, Chen Zhang, Guangyu Sun, Guohao Dai, Runsheng Wang, Zhigang Ji, Ru Huang

Presenter: **Shiyu Xia**, Shanghai Jiao Tong University

Abstract: Recent advances in DRAM technologies and large-dataset applications in data centers make both academic and industrial researchers eager to explore DRAM's novel usage and cross-disciplinary DTCO (design and technology co-design) spaces, as illustrated by recent studies of the PIM (Processing-In-Memory) or RowHammer effect etc. This evolving landscape has created a pressing need for systematic testing and validation of those emerging DTCO studies. However, previous DRAM simulators have lacked joint modeling of device and architecture, impeding effective simulation of these DTCO designs. To address this gap, we introduce DATIS (DRAM Architecture and Technology Integrated Simulator), a tool that effectively connects architectural design and the complexities of DRAM technology. DATIS addresses two critical challenges: abstracting technology intricacies and establishing connections between architectural activities and device-level process structures. This versatile tool empowers researchers to unlock the latent capabilities of DRAM and provides manufacturers with a platform to experiment with new processes and architecture co-design. To the best of our knowledge, DATIS is the first DRAM simulator in academia that integrates architecture and technology modeling. We build DATIS upon Ramulator, a well-known open source DRAM simulator for architecture-level modeling, and thus it can support a wide range of DRAM specifications, including DDRx, LPDDR5, GDDR6, and HBM2\&3 etc. Our experiments demonstrate DATIS's efficacy and precision through three compelling case studies, addressing pivotal facets of DRAM technology, including storage, reliability, and computation.

17:00-17:20 | Paper ID: 231

Title: A Survey of Standard Cell Layout Design

Author(s): Jie Zhou, Zhiyuan Luo, Zhien Li, Huiqing You, Mingxiao He, Zhenyu Zhao

Presenter: **Zhiyuan Luo**, National University of Defense Technology

Abstract: Standard cells serve as fundamental building blocks in the integrated circuit (IC) design flow. The efficiency and quality of standard cell layout design have consistently been a major research focus in both academia and industry. With design-technology co-optimization (DTCO) playing an increasingly critical role in advanced technology nodes, standard cell layout design is undergoing a paradigm shift from traditional approaches to system-level optimization. In this paper, we systematically review the evolution of standard cell layout design, categorizing its development into three distinct phases: manual design era, automated design era and the design-technology (DT) co-design era. Building upon this historical framework, we first introduce the general flow of standard cell layout design during the era of manual design. This flow comprises four key stage: schematic drafting, stick diagram design, layout drafting, and physical verification. Subsequently, we analyze the core challenge in transitioning from manual to automated design: formulating the transistor placement and in-cell routing as a solvable optimization problem through constraint modeling. We then provide a comprehensive review of the methods employed in related work over the past four decades, encompassing graph-based algorithms, heuristic algorithms, constraint solvers, and AI-based methods. Finally, we delve into the emerging design paradigms of the DT co-design era, offering a perspective on the future of standard cell design. This perspective encompasses: concurrent cell-level and system-level optimization; finer-grained modeling and integrated design flows; specialized, custom cell library design and AI-assisted intelligent design.

17:20-17:40 | Paper ID: 232

Title: Efficient SRAF Generation via Diffusion Models

Author(s): Minjie Bi, Yang Luo, Xiaoxiao Liang, Zhengzhou Gu, Jinbin Deng, Binwu Zhu, Yuzhe Ma
Presenter: **Minjie Bi**, The Hong Kong University of Science and Technology (Guangzhou)
Abstract: In semiconductor manufacturing, optical proximity correction and sub-resolution assist features (SRAF) are critical techniques for achieving high-fidelity wafer images, especially as semiconductor device critical dimensions shrink. However, traditional SRAF generation methods often face challenges in scalability, adaptability, and efficiency. This paper introduces a novel method that uses a conditional generative diffusion model for SRAF generation to improve efficiency and flexibility. We treat the SRAF generation task as an image-to-image translation problem, converting the input layout to include optimal assist features. Experimental results show that our proposed approach achieves a 5.57× speed-up over commercial tools while maintaining comparable accuracy in terms of edge placement error and process variation band.

17:40-18:00 | Paper ID: 194
Title: GMUNet-ILT: A lightweight MLP-based network for Inverse Lithography Technology
Author(s): Ke Wang, Kun Ren, Zebang Lin, Dawei Gao, Yongyu Wu, Shibin Xu
Presenter: **Ke Wang**, Zhejiang University
Abstract: With the continuous scaling down of critical dimension (CD) in advanced integrated circuits, Resolution Enhancement Techniques (RETs) are employed to improve the printing performance in lithography processes. Inverse lithography, a widely studied RET, precisely controls the printed images on wafers. As a type of computational lithography, inverse lithography often incurs significant computational costs. Therefore, this paper proposes a lightweight and fast deep learning convolutional network architecture for computational lithography, which is based on an improved U-Net incorporating shifted-window multi-layer perceptron and Ghost modules. Our approach achieves relatively low mask error and a runtime of less than 5 seconds.

TECHNICAL SESSIONS

TS 14. Efficient Parameter Extraction and Modeling Techniques

16:00-18:00 | May 10, 2025 @ Snow White 1

Session Chair: Zichao Ma, South China University of Technology

16:00-16:20 | Paper ID: 25

Title: Multi-Objective Bayesian Target Interval Optimization for Semiconductor Process Parameters

Author(s): Xiao Yang, Xingyu Qin, Yujie Zhang, Jianwang Zhai, Kang Zhao

Presenter: **Xiao Yang**, Beijing University of Posts and Telecommunications

Abstract: Semiconductor manufacturing is becoming increasingly complex, making optimization of process parameters both challenging and costly. In Physical Vapor Deposition (PVD) processes, high-dimensional nonlinear relationships between input parameters and output performance exacerbate these difficulties, particularly under conditions of limited data and multi-objective constraints. To tackle these challenges, we propose a Bayesian Optimization (BO) framework integrating Sparse Multi-task Gaussian Process (SMTGP) and Probability-guided Interval Search Mechanism (PRISM) for process parameter optimization. By incorporating a Multi-input Multi-output (MIMO) Predictor with Soft Physical Constraints, the framework effectively combines physical priors with learning-based modeling, enhancing predictive accuracy and reliability in low-data scenarios. Experimental evaluations across various scenarios demonstrate that the proposed method outperforms Random Search (RS) and classical BO in both efficiency and reliability.

16:20-16:40 | Paper ID: 229

Title: Task Scheduling and Temperature Optimization Co-Design for Multi-Core Embedded Systems

Author(s): Jingxi Yao, Lei Mo, Jie Han, Dan Niu

Presenter: **Lei Mo**, Southeast University

Abstract: The high integration and power density of multi-core processors increase energy consumption and chip temperatures, affecting reliability and accelerating aging. Effective energy and temperature management is crucial to maintaining performance and extending processor lifespans. This paper proposes a real-time task scheduling approach using Dynamic Voltage and Frequency Scaling (DVFS) to optimize energy and temperature in embedded Multi-Processor System-on-Chip (MPSoC) platforms. We introduce a thermal model and develop a Mixed-Integer Nonlinear Programming (MINLP) model to optimize task allocation and scheduling, considering real-time, dependency, non-overlapping, and thermal constraints. To simplify the problem, we linearize the MINLP model into a Mixed-Integer Linear Programming (MILP) model. A Genetic Algorithm (GA)-based method is also proposed to improve scalability. The GA method accounts for task allocation, processor selection, and thermal constraints, while prioritizing lower execution frequencies to reduce energy use. Simulation results show that the proposed approach effectively reduces energy consumption and computation time, which is suitable for complex multi-core platforms.

16:40-17:00 | Paper ID: 230

Title: Optimization of N/P Performance Matching through Adjusting Extension Region Doping Concentration for Vertical Gate-All-Around FETs

Author(s): Xinlong Guo, Tao Liu, Ziqiang Huang, Lewen Qian, Meicheng Liao, Min Xu, David Wei Zhang

Presenter: **Xinlong Guo**, Fudan University

Abstract: A novel vertical gate-all-around FET (VGAAFET) structure based on the Si/SiGe/Si/SiGe/Si epitaxial stacks is proposed for integrating the controllable gate and spacer lengths, as well as self-aligned junctions. In

the proposed VGAAFET structure, SiGe layers served as extension regions form the doping pocket between the Si source/drain (S/D) and Si channel in pFET due to the higher solid solubility of boron in SiGe. Optimization of the doping concentration in the pFET extension regions has been demonstrated to enhance the saturation current of the pFET by 23% and improve the n/p current ratio from 1:0.74 to 1:0.91 when compared to undoped extension regions. To further investigate the performance improvement of the VGAAFET-based ring oscillator (RO) by adjusting the doping concentration in the extension regions, the design-technology co-optimization (DTCO) platform is established. An enhancement of 17% in frequency and a reduction of 12% in energy-delay product (EDP) have been achieved when the doping concentration of the pFET extension regions is the same as that of the S/D.

17:00-17:20 | Paper ID: 235

Title: Efficient Parameter Extraction for GaN HEMTs Using Rational Function Assisted Neural Network

Author(s): Zhenhai Cui, Guangxin Guo, Yifan Tai, Cong Li, Ziyue Zhao, Hailang Wang, Hailong You

Presenter: **Zhenhai Cui**, Xidian University

Abstract: This work proposes a novel method integrating Rational Function Preprocessing (RFP) with Artificial Neural Network (ANN) to efficiently extract ASM-HEMT model parameters from S-parameters of Gallium Nitride High Electron Mobility Transistor (GaN HEMT) devices. Compared to conventional ANN parameter extractors, this method represents a significant advancement in the field. The innovation lies in developing an advanced rational function model specifically designed to accurately capture the complex high-dimensional frequency characteristics of GaN HEMT S-parameters. By effectively preserving the essential frequency response characteristics, it successfully eliminates interference from redundant S-parameters. Experimental results highlight substantial performance improvements, with training time reduced from 9035 seconds to 670 seconds under comparable error conditions, achieving a 92.6% reduction. The Root Mean Square Percentage Error (RMSPE) for parameter extraction decreases from 7.55% to 4.13%, representing a 45% optimization in accuracy under the same neural network architecture. This method holds significant engineering as 5G base stations and Rfpower amplifiers.

17:20-17:40 | Paper ID: 237

Title: Experiment and TCAD Hybrid-data-Driven Modeling of Advanced Node GAAFETs by Transfer Learning

Author(s): Yuhan Jiang, Haoqing Xu, Kun Luo, Qingzhu Zhang, Huaxiang Yin, Zhiqiang Li, Zhenhua Wu

Presenter: **Yuhan Jiang**, Institute of Microelectronics, Chinese Academy of Sciences

Abstract: Gate-All-Around transistors for advanced technology nodes present significant simulation challenges due to their intricate 3-dimensional structures and diverse process and device configurations. The scarcity of experimental data, constrained by high costs and time, further complicates the accurate calibration of robust TCAD models. This study introduces a novel neural network technique that synergizes experimental and TCAD hybrid data with transfer learning. By training a base model on a comprehensive GAAFET simulation dataset and fine-tuning it with minimal experimental data, the method reduces dependency on experimental data by over 80%. Results demonstrate a 98% improvement in predictive accuracy and a substantial reduction in calibration time compared to conventional methods. This approach highlights the potential to significantly enhance the efficiency and accuracy of advanced node device design and development.

17:40-18:00 | Paper ID: 221

Title: Compact Model of Superparamagnetic Tunnel Junction Controlled by Spin-Orbit Torque

Author(s): Chaoyue Zhang, Yefan Xu, Yu Gong, Shouzhong Peng, Yue Zhang, You Wang

Presenter: **Chaoyue Zhang**, Nanjing University of Aeronautics and Astronautics

Abstract: Superparamagnetic tunnel junction (SMTJ), characterized by thermally driven random magnetization switching, offer novel pathways for high-sensitivity magnetic sensing and true random number generation. In

this study, we developed a compact model based on magnetization dynamics and electrical characteristics for SMTJs modulated by spin-orbit torque (SOT). The temporal evolution of the magnetic moments in the free layer (FL) is described by a revised Landau-Lifshitz-Gilbert (LLG) equation, which accounts for thermal noise effect. A voltage-dependent tunneling magnetoresistance (TMR) model is introduced, thereby establishing a robust framework for circuit simulation. The model is developed by using the Verilog-A language, and the accuracy of the model was verified through simulations. The simulation results indicate that the magnetization state retention time of SMTJ is positively correlated with the thermal stability factor, and the external voltage can modulate the probability distribution of magnetization direction. This research provides theoretical support and design references for the application of superparamagnetic devices in low-power random circuits and high-precision sensors.

TECHNICAL SESSIONS

TS 15. Large Language Models and Next-Generation EDA Tools

16:00-17:40 | May 10, 2025 @ Snow White 2

Session Chair: **Cheng Liu**, Institute of Computing Technology, Chinese Academy of Sciences

16:00-16:20 | Invited Talk

Bing Li

University of Siegen

Bio.: Bing Li is a professor with the University of Siegen, Siegen, Germany, since July 2024. Before that, he worked at TU Munich for about 20 years. His research interests include AI-assisted EDA, circuit and system architectures, and emerging technologies such as RRAM and optical accelerators for neural networks.

Title: LLM-Aided HLS Repair and Testbench Generation

Abstract: With the rapidly increasing complexity of modern chips, hardware engineers are required to invest more efforts in tasks such as circuit design and verification. These workflows often involve continuous modifications, which are labor-intensive and prone to errors. Therefore, there is an increasing need for more efficient and cost-effective Electronic Design Automation (EDA) solutions to accelerate new hardware development. Recently, large language models (LLMs) have made significant advancements in contextual understanding, logical reasoning, and response generation. Since hardware designs and intermediate scripts can be expressed in text format, it is reasonable to explore whether integrating LLMs into EDA could simplify and fully automate the circuit design workflow. This talk discusses the application of LLMs in HLS (High-Level Synthesis) code repair and testbench generation as well as future challenges and opportunities.

16:20-16:40 | Paper ID: 184

Title: MALTS: A Multi-Agent Large Language Model-Based Layout-to-TCAD Structure Synthesizer

Author(s): Jiaqi Dou, Jianing Zhang, Bingyi Ye, Yang Shen, Xiaojin Li, Yanling Shi, Yuhang Zhang, Yabin Sun

Presenter: **Jiaqi Dou**, East China Normal University

Abstract: The demand for efficient 3D modeling in Technology Computer-Aided Design (TCAD) simulations has surged, driven by the need for rapid device performance evaluation and Design Technology Co-Optimization (DTCO). Traditional TCAD modeling involves time-consuming process emulation and complex script editing, which limits the scope within single-device simulations and hinders scalability. To address these challenges, this paper introduces MALTS, a multi-agent large language model-based layout-to-TCAD structure synthesizer. The proposed framework takes industrial layout files (e.g., GDSII) and process information as inputs, and directly generates simulation-ready definitions in standard TCAD syntax, eliminating the need for iterative process emulation and manual script adjustments typically required in conventional workflows. By decomposing the synthesis process and assigning each phase to a specialized LLM agent, MALTS mitigates the ``long-context forgetting'' problem, enabling efficient generation of complex structures and gate-level TCAD models. Experimental results demonstrate that the proposed framework provides an automated solution for analyzing the impact of various physical layout designs and process details on electrical characteristics, facilitating rapid design space exploration in the DTCO process.

16:40-17:00 | Paper ID: 202

Title: Finetuned Decision Transformer with Tree Search for Logic Synthesis Optimization

Author(s): Chenyang Lv, Chenyu Xu, Zhezhi He, Chunyang Feng

Presenter: **Chenyu Xu**, Shenzhen Giga Design Automation Co., Ltd.

Abstract: Logic synthesis (LS) involves the conversion of high-level circuit descriptions into gate-level netlists. However, identifying the optimal primitive sequences (PS) for this transformation is a formidable challenge due to the expansive design space. While machine learning has been employed to address this issue, existing methods often necessitate extensive training or result in high computational costs. GPT-LS revolutionized LS optimization by reframing it as a sequence generation problem and leveraging a pre-trained transformer with offline reinforcement learning to generate PS effectively. In this work, we integrate tree search and model fine-tuning to enhance the transferability and performance of GPTLS, particularly in unseen cases, which significantly improves efficiency and effectiveness with minimal runtime increase, establishing a new standard in LS optimization. Experimental results demonstrate that, after just a few rounds of fine-tuning, it outperforms all previous methods, including state-of-the-art Bayesian optimization techniques and long-running random searches.

17:00-17:20 | Paper ID: 242

Title: AnaSizeCoder: Code Generator for Analog Integrated Circuit Sizing Automation via Large Language Model

Author(s): Wenzhao Sun, Yanan Han, Bijian Lan, Qing Peng, Jing Wan

Presenter: **Wenzhao Sun**, Fudan University

Abstract: This study proposes a task-driven approach AnaSizeCoder that utilizes the large language model (LLM) Qwen2.5 to automatically generate optimization code for transistor sizing in analog integrated circuits (IC). Traditional optimization techniques often require manual code adjustments when faced with different optimization objectives and constraints, limiting their flexibility and efficiency in complex design tasks. To address this issue, we fine-tuned the Qwen2.5 model using LoRA (Low-Rank Adaptation) technology, enabling it to generate high-quality optimization code based on user-provided natural language requirements. We constructed a dataset comprising user requirements, summarized information, and corresponding optimization code, and consolidated all data for fine-tuning. The model was trained on 3 analog circuits, covering different optimization goals and constraints. Experimental results show that the fine-tuned model significantly improves code generation accuracy, with the best performance observed at the 4th training epoch (Epoch 4). In terms of generating summarized information, the accuracy reached 100%, while for code generation, the accuracy was above 97% across 3 different circuits. Additionally, by implementing the LDO (Low Dropout Regulator) circuit, we validated the code generated by AnaSizeCoder can successfully run and achieve the optimal Pareto frontier. Our approach enhances the automation and efficiency of analog IC design, reduces human intervention, and accelerates the design process.

17:20-17:40 | Paper ID: 15

Title: ChaTCL: LLM-Based Multi-Agent RAG Framework for TCL Script Generation

Author(s): Yibo Rui, Yuanhang Li, Rui Wang, Yanxiang Zhu, Ruiqi Chen, Zhixiong Di, Ming Ling, Xi Wang

Presenter: **Yibo Rui**, National ASIC System Engineering Technology Research Center, Southeast University

Abstract: Manually generating Tool Command Language (TCL) scripts is time-consuming and error-prone. Although large language models (LLMs) show promise in automating TCL script generation, they struggle with complex EDA tasks. They often fail to meet practical requirements and face compatibility issues across multiple tools. To address these limitations, we introduce ChaTCL, a multi-agent Retrieval-Augmented Generation (RAG) framework based on LLMs. Our contributions include: (1) creating fine-tuned datasets (NondomainT and DomainT) for TCL-specific LLMs, (2) designing a TCL-specific RAG framework with one-to-one retriever-database mapping to reduce hallucinations, and (3) implementing a multi-agent system that interprets user prompts and autonomously selects agents for script generation. Evaluated using TCLEval, ChaTCL outperforms models like ChatGPT-4.0-o and OpenAI o1-preview in generating accurate scripts across diverse tools and design stages.

TECHNICAL SESSIONS

TS 16. Power Modeling, Analysis, and Thermal Management

10:40-12:00 | May 11, 2025 @ Sleeping Beauty 1/2

Session Chair: Zhiyao Xie, The Hong Kong University of Science and Technology

10:40-11:00 | Paper ID: 11

Title: An LSTM-Based ESL Power Prediction Model Design Optimization Method

Author(s): Zhishuai Wei, Kang Li, Chenglong Xu, Shuo Han, Heqian Hou, Vazgen Melikyan

Presenter: **Zhishuai Wei**, Xidian University

Abstract: With the increasing complexity of functionality and scale in network processing and AI chips, power has become a critical constraint in the design of future processor architectures. Therefore, accurately quantifying processor power during the early stages of design and at higher levels of abstraction is crucial. Particularly in scenarios such as network packet switching, where time-series feature dependencies are significant, fully exploiting and utilizing temporal correlations can significantly enhance power prediction performance. This article proposes an ESL power prediction model that extracts key features from ESL model simulations and architectural design parameters, combined with a Long Short-Term Memory (LSTM) to construct an architecture-level power prediction model. Validation was performed on high-throughput network switching chips. The results show that the proposed model effectively improves the accuracy of ESL power prediction, achieving an average prediction error of less than 5% for both component-level and system-level power, with the best case reaching as low as 1.8%.

11:00-11:20 | Paper ID: 152

Title: GPU Acceleration of A High-precision Stochastic Solver for Steady-state Thermal Analysis with Robin Boundary Conditions

Author(s): Yonghan Luo, Yuyan Wang, Zhixuan Dong, Changhao Yan, Zhaori Bi, Keren Zhu, Shengguo Wang, Xuan Zeng

Presenter: **Yonghan Luo**, Fudan University

Abstract: Thermal analysis is crucial for modern chip design. The Path Integral Random Walk (PIRW) solver is a high-precision and highly parallel stochastic method-based solver, which is accurate for steady-state thermal analysis with mixed boundary conditions. However, it requires a large number of paths to ensure a result with small variance, as well as massive jump steps to ensure the convergence of the accumulated temperature. This results in limited performance when executed on CPUs. To address these limitations, we have developed a GPU-accelerated implementation of PIRW that capitalizes on the massive parallelism and advanced scheduling capabilities of modern GPUs. Our implementation enables large-scale parallel computation of random walk paths, significantly enhancing computational efficiency. Furthermore, by leveraging the algorithm's inherent characteristics, we have developed a fitting algorithm that substantially reduces the number of path steps required for convergence. The experiment shows that, compared to multi-threaded version on CPU with 80 threads, the PIRW on NVIDIA A800 GPU with step-reducing fitting technology achieves a speed up of 64.1x.

11:20-11:40 | Paper ID: 165

Title: Mutual Information-Driven Thermal Sensor Planning Method Assisting On-chip Temperature Monitoring at Device-Level Granularity

Author(s): Wangyong Chen, Weizhi Li, Zhenming Li, Linlin Cai

Presenter: **Weizhi Li**, Sun Yat-sen University

Abstract: On-chip temperature monitoring is becoming increasingly significant in preventing local over-heating and managing the reliability of electronic system, especially in 3D-stacked chips. A cost-effective thermal sensor planning method that assists in accurate temperature tracking in different application scenarios is highly desired. Therefore, we propose a mutual information (MI)-based technique to allocate the limited thermal sensors while maintaining a high level of accuracy in full thermal maps (resolution: <1 K). The thermal analysis workflow to assist in the hotspots monitoring from the standard cell level down to the device level is presented, aiming at effectively capturing the time-varying and scenario-dependent thermal responses with finer granularity. The results suggest that the proposed method exhibits lower errors compared to existing approaches that use the same number of thermal sensors, and also shows great robustness in unknown scenarios.

11:40-12:00 | Paper ID: 180

Title: Pre-Silicon Power Side-channel Leakage Assessment Through Quantitative Information Flow Analysis

Author(s): Xingxin Wang, Huisi Zhou, Jiacheng Zhu, Weihao Fan, Wei Hu

Presenter: **Xingxin Wang**, Northwestern Polytechnical University

Abstract: Power side-channels can cause leakage of cryptographic keys and pose a significant threat to hardware security. Although post-silicon power side-channel analysis methods are generally effective in leakage assessment, discovering side-channels after fabrication is too late, since security vulnerabilities in chips are difficult to eliminate or patch. This work aims to develop a pre-silicon power side-channel leakage assessment method that allows the evaluation of power leakage in the early hardware design and verification stages through quantitative information flow analysis. The key observation is that the distribution of taint labels can reveal power consumption characteristics. The paper constructs fine-grained precise information flow models (IFM) for cryptographic hardware designs for calculating taint labels. It further employs Shannon entropy to measure the distribution of taint labels related to secret key bits and quantify power side-channel leakage. Experimental results using AES and SM4 core designs show that our method can precisely identify modules with power side-channel security vulnerabilities and quantitatively assess the degree of leakage.

TECHNICAL SESSIONS

TS 17. Advanced Test Methodologies and DFT Techniques

10:40-12:00 | May 11, 2025 @ Sleeping Beauty 3

Session Chair: **Huawei Li**, Institute of Computing Technology, Chinese Academy of Sciences

10:40-11:00 | Invited Talk

Hans-Joachim Wunderlich

University of Stuttgart

Bio.: Hans-Joachim Wunderlich is Professor Emeritus of the University Stuttgart and a Life Fellow of IEEE. He received the diploma degree in mathematics from the University of Freiburg, Germany, in 1981 and the Dr. rer. nat. (Ph.D. degree) from the University of Karlsruhe in 1986. Since 1991, he has been a full professor. From 2002 to 2018, he was the director of the Institute of Computer Architecture and Computer Engineering at the University of Stuttgart, Germany. He has been associate editor of various international journals and organizer of a variety of IEEE conferences on design, test and fault tolerance of electronic systems. He has published 15 books and book chapters and around 330 reviewed scientific papers in journals and conferences. His research interests include test, reliability, fault tolerance and design automation of microelectronic systems.

Title: In-Field Deterministic Logic BIST under PVT-Variations

Abstract: Safety-critical systems in automotive, air or space applications integrate the infrastructure for deterministic logic built-in self-test (DLBIST) to be used in the field periodically and at power-on and power-off. The BIST has to be effective for any admissible instance subject to process variations and under any admissible condition due to voltage and temperature fluctuations. This contribution discusses DLBIST solutions which optimize fault coverage, test storage requirements and test application times simultaneously.

11:00-11:20 | Paper ID: 114

Title: DFTS: An Efficient Design-for-Test Flow for Scan Design

Author(s): Jun Gao, Mingjun Wang, Jiangwang Liu, Wenjie Li, Zizhen Liu, Jing Ye, Huawei Li

Presenter: **Mingjun Wang**, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences

Abstract: Modern integrated circuit (IC) development faces increasing demands for test coverage, cost efficiency, and reduced turnaround time, particularly with the shift to nanometer technology nodes and heterogeneous 3D integration. To address these challenges, we propose DFTS, a holistic Design-for-Test (DFT) methodology for scan design, consisting of five key components: netlist parsing, module uniquify operations, minimal MUX-based repairs of design rule checking (DRC) violations, balanced scanchain construction, and clean circuit dumping for automatic test pattern generation (ATPG) or fault simulation. DFTS employs hierarchical parsing to capture clock, set, and reset domains accurately while minimizing redundant module definitions through unique operations. A selective DRC-violation repair mechanism efficiently inserts MUXes only where necessary, avoiding overfixing in constant-gated or properly configured paths. Additionally, a multi-domain scan-chain balancing algorithm evenly distributes scan cells across clock domains; switching activities were shared over several clock domains, reducing shift cycles. Experiments on CPU-like netlists demonstrated significant reductions in unnecessary MUX insertions and a runtime speedup of 3×–43× compared to a leading commercial DFT solution. These results highlight the scalability and competitiveness of

the proposed methodology, making it a robust solution for addressing DFT challenges in scan design of modern IC designs.

11:20-11:40 | Paper ID: 118

Title: RDT: An Optimized Automatic Test Pattern Generation Method Based on Robust Decision Tree

Author(s): Dengjie Mao, Dapeng Yan, Zhipeng Gao, Zhiming Liu, Haiping Huang, Zhikuang Cai

Presenter: **Dapeng Yan**, Nanjing University of Posts and Telecommunications

Abstract: Automatic Test Pattern Generation (ATPG) is a crucial technology in digital circuit testing. However, as circuit complexity increases, traditional methods face significant challenges, including inefficiency and resource waste caused by excessive backtracking. This paper presents an optimized ATPG method based on robust decision trees to mitigate backtracking and improve overall performance. The approach involves constructing a decision tree to learn the rich historical backtracking data generated during the FAN ATPG process, incorporating a negative exponential loss function to reduce the impact of noisy data on model quality. The trained model is then used to guide backtracking decisions in ATPG, thereby enhancing efficiency. Experimental results on ISCAS89 and ISCAS85 benchmark circuits demonstrate that, compared to deep learning-optimized ATPGmethods, the proposed approach reduces backtracking frequency by 24% and test pattern count by 25%, while maintaining comparable test quality.

11:40-12:00 | Paper ID: 127

Title: GEMMHeal: An Efficient Self-repairing Architecture for Matrix Multiplication

Author(s): Yuxuan Qiao, Changxu Liu, Hao Zhou, Yifei Feng, Yifan Song, Junjie Zuo, Fan Yang

Presenter: **Changxu Liu**, Fudan University

Abstract: In modern machine learning models like Transformers, matrix multiplication dominates most computation. Specific hardware often uses large-scale PE arrays, such as systolic arrays, to accelerate this process. However, these extensive PE arrays tend to experience high fault rates, with cumulative errors in matrix multiplication potentially impacting final algorithmic outcomes. We propose GEMMHeal, a self-repairing, systolic-array-like architecture optimized for matrix multiplication. This architecture optimizes the matrix multiplication array design and data flow in the buffer while decoupling the error correction (EC) core from the array. The EC core operates as an independent computation unit, maintaining resource efficiency and avoiding performance degradation due to the spatial locality of faults. Additionally, our proposed design incorporates redundancy within the EC core, allowing it to self-repair and thus further improve fault tolerance. GEMMHeal is implemented in a 32nm process to demonstrate its area and physical achievability. A single EC core occupies only 1.8% of the area while effectively repairing up to 6.3% of faulty PEs, all while maintaining overall performance. By accounting for potential faults within the EC core, our redundant design achieves an average improvement of 31% in the EC core normal rate compared to non-redundant designs when the computation cell fault rate is within 15%.

TECHNICAL SESSIONS

TS 18. Device Compact Modeling and Process Simulation

10:40-12:00 | May 11, 2025 @ Sleeping Beauty 5

Session Chair: Lining Zhang, Peking University ShenZhen Graduate School

10:40-11:00 | Invited Talk

Lan Wei

University of Waterloo

Bio.: Prof. Lan Wei received her B.S. in Microelectronics from Peking University, China (2001), M.S and Ph. D. in Electrical Engineering from Stanford University, USA (2007 and 2010, respectively). She is currently an Associate Professor at the University of Waterloo, Canada. She has intensive experience in device physics-based compact modeling including silicon and wide-bandgap semiconductor technologies, device-circuit interactive design and optimization, integrated nanoelectronic systems with low-dimensional materials, cryogenic CMOS device modeling and circuit design for quantum computing. Dr. Wei is the co-developer of the MIT Virtual Source GaN HEMT (MVSG) Compact Model, an Industry Standard approved and supported by the Compact Model Coalition for GaN HEMT compact model. She has authored/co-authored more than 90 peered reviewed publications and served on the technical program committees including IEDM, ICCAD, DATE, ISQED, BCICTS, ISPSD, etc.

Title: Formulation and Applications of Industry-standard MVSG GaN HEMT Compact Model

Abstract: Given its high mobility, high breakdown voltage and decent thermal conductivity, GaN HEMT devices are a front-runner for the next generation power RF applications and power electronics applications. With commercial roll-out of GaN technology, development of accurate, scalable and efficient compact model is essential. The MIT Virtual-source Gallium Nitride (MVSG) model is one of the two industry-standard compact models for GaN HEMTs.

This presentation will provide a brief overview of the physics-based MVSG GaN HEMT compact model, including the model formulation and various features. Its recent progress for RF GaN and power GaN devices will also be presented with application examples, showing the potentials of this physics-based compact model.

11:00-11:20 | Paper ID: 40

Title: HiRL-DCMPE：A Combined HiMOSS and RL Framework for Device Compact Model Parameter Extraction

Author(s): Ziyan Zhou, Gongteng Xiao, Shisheng Xiong, Zhaori Bi, Fan Yang, Xuan Zeng, Ye Lu

Presenter: **Ye Lu**, Fudan University

Abstract: The relentless scaling of semiconductor device technology has significantly increased the complexity and computational demands of device compact model (DCM) parameter extraction and model creation. The extraction workflow typically needs to simultaneously optimize hundreds of interdependent parameters while meeting stringent requirements for both computational efficiency and model physical accuracy. In this work, a new method that combines HiMOSS with RL algorithms for DCM parameter extraction is proposed. Specifically, we (i) propose HiRL-DCMPE, a novel algorithm that combines a modified Bayesian optimization and reinforcement learning. This framework narrows down the high-dimensional search space in the early stage and subsequently performs fine-grained optimization locally in the later stage. This not only improves the performance but also enhances the efficiency of the automated DCM parameter extraction; (ii) conduct experiments of parameter extraction task for both BSIMCMG and BSIMSOI models, and more than 100

parameters are extracted at once. It is shown that the RMSE of the created model output v.s. target data is < 5%, satisfying the needs of practical usage. In addition, the results outperform the benchmark algorithms by at least 20% in terms of RMSE value; and (iii) Overall, this framework improves the search efficiency and facilitates the optimal solution for complex DCM parameter extraction tasks. It takes at least 11.8% less time compared to the benchmark algorithm to reach the same accuracy level. These results demonstrate the great potential of HiRL-DCMPE for future DCM parameter extraction purpose.

11:20-11:40 | Paper ID: 95

Title: APEX: Automating Parameter Extraction of Compact Models with Differential Neural Network Approximation

Author(s): Jianing Zhang, Jiaqi Dou, Yang Shen, Bingyi Ye, Xiaojin Li, Yanling Shi, Yuhang Zhang, Yabin Sun

Presenter: **Jianing Zhang**, East China Normal University

Abstract: The traditional compact model parameter extraction highly depends on engineers' expertise, leading to a time-consuming and iterative process. To address the above issue, this paper proposes an automatic parameter extraction method for compact models, APEX. The proposed APEX framework adopts an artificial neural network (ANN) method as an approximation of compact models using model parameters as inputs and IV/CV data as outputs. The model parameters are efficiently extracted using an automatic differential mechanism based on the ANN-approximated compact model. Experimental results demonstrate that our proposed framework achieves good fitting accuracy and scalability across device structures when evaluating GAA and FinFET devices. A fitting error of less than 4% is achieved on the open-source benchmark.

11:40-12:00 | Paper ID: 132

Title: MOIL: An Efficient Multi-objective Optimization Framework for SRAM Cell with Incremental Learning

Author(s): Baokang Peng, Guoyao Cheng, Jiajun Qiu, Runsheng Wang, Lining Zhang

Presenter: **Baokang Peng**, Peking University

Abstract: This paper proposes MOIL, an efficient multi-objective optimization framework for SRAM design that combines neural network (NN) surrogate modeling with NSGA-II evolutionary algorithms. The framework features: 1) An NN surrogate model employing a two-phase training strategy — initially trained on Latin Hypercube Sampling data and progressively refined through incremental learning cycles — achieving 99.83% prediction accuracy on critical SRAM metrics (read/write delay, SNM, leakage power) while eliminating iterative SPICE simulations; 2) An adaptive NSGA-II optimizer incorporating dynamic crowding distance calculation to effectively explore 5-dimensional device parameters (Fin width/height, Lg, PHIG) and generate Pareto-optimal solutions. Experimental results demonstrate MOIL's superior efficiency with 20.8× faster decision-making and 13.7× speedup over Bayesian optimization method, while maintaining solution diversity (hypervolume ratio of 3.52). The framework establishes a robust methodology for rapid SRAM evaluation and optimization in advanced technology nodes.

TECHNICAL SESSIONS

TS 19. Emerging Technologies and Applications in EDA

10:40-11:40 | May 11, 2025 @ Snow White 2/3

Session Chair: Shixi Chen, Huawei Design Automation Lab, Hong Kong

10:40-11:00 | Invited Talk

Pei-Hsin Ho

Shanghai UniVista Industrial Software Group Co., Ltd

Bio.: Dr. Pei-Hsin Ho serves as the Chief Technology Officer (CTO) of UniVista Industrial Software Group, where he oversees R&D of Emulation, AI in EDA, and Digital Implementation. Prior to his current role, Dr. Ho held the position of Synopsys Fellow, where he led research and development teams of Synopsys Emulation, Physical Design, and Formal Verification products. Dr. Ho holds 15 U.S. and Chinese patents and authored over 35 peer-reviewed papers with 11,000+ citations (based on Google Scholar).

Title: Domestic EDA Tools and IP Solutions: Accelerating Breakthroughs in Chinese AI Chip Design

Abstract: The emergence of AI-driven intelligent computing has spurred an exponential increase in demand for compute power. At the same time, shifting geopolitical conditions and evolving supply chain dynamics are posing unprecedented challenges to the design and manufacturing of Chinese AI chips. In response, UniVista has introduced a comprehensive solution that integrates advanced EDA tools and high-performance IPs to enable software-driven and advanced-packaging–driven AI chip designs. In this talk, we will share UniVista's latest innovations, including: (1) cutting-edge EDA tools, such as the UVHS emulator for system-level functional and performance verification, the Chiplet Explorer for advanced packaging design, and the UDA AI-powered digital design platform and (2) Advanced IP solutions, including RDMA, UCIe, and HBM. We will demonstrate how these technologies, working together, can help accelerate the design and innovation of Chinese AI chips to meet compute-power demands.

11:00-11:20 | Paper ID: 17

Title: Electrothermal Simulation and Vertical Interconnect Planning for Integrated Chiplets

Author(s): Siyuan Miao, Lingkang Zhu, Wenkai Yang, Teng Lu, Yanze Zhou, Chen Wu, Zhiping Yu, Ting-Jung Lin, Lei He

Presenter: **Siyuan Miao**, University of California, Los Angeles

Abstract: Chiplets are emerging as novel solutions for high-performance AI computing processors. Vertical interconnects (VICs) including μbumps, C4 bumps and through-silicon vias (TSVs) in chiplets are critical as they not only carry signals and power supplies but also transfer heat efficiently. Due to the need of fine-grained VIC modeling, existing thermal tools are ineffective for VIC-embedded chiplets. Moreover, electrothermal analysis in previous architectural simulators does not consider temperature dependence for short-circuit power, which is non-trivial in our experiments. To address the above problems, this paper proposes SYSgen, a framework for accurate, location-based temperature dependent power profiling and VIC planning for integrated chiplets. SYSgen achieves a 97.77× speedup with a maximum error below 1.2°C when the chiplet temperature is around 100°C compared to COMSOL. It also reduces VIC number by 21.7% and 12.4% compared to two existing papers with same constraints on signal and power routing and maximum temperature.

11:20-11:40 | Paper ID: 227

Title: PHAROS: An Adaptive Optimization and DRC Correction Tool for Accurate Photonic Design Automation

Author(s): Yichi Zhang, Zhaoyang Xin, Guochang Lin, Qisheng Yang, Tian-Ling Ren
Presenter: **Qisheng Yang**, Hunan University

Abstract: The rapid advancement of photonic computing has highlighted its potential for high-speed, low-power parallel computation. Nonetheless, traditional inverse design for photonic integrated circuits (PICs) face challenges, such as irregular structural patterns and the necessity for manual design rule checks (DRC). These factors contribute to extended design cycles and diminished efficiency. To address these problems, this work proposed PHAROS, an adaptive optimization tool for automated photonic design automation. PHAROS employs adjoint-method gradient optimization. It integrates adaptive filtering and quantization mechanisms. These features enable the simultaneous optimization of electromagnetic performance and adaptation to manufacturing constraints. Then, a feedback system further enabled automatic DRC correction, ensuring compliance with foundry-specific process design kits (PDKs). Simulation results demonstrated the PHAROS's robustness across diverse PDKs nodes and pixel resolutions. By automating the workflow from objectives to manufacturable layouts, PHAROS established a promising path for future optical design automation (PDA).

TECHNICAL SESSIONS

TS 20. Advanced Analog Simulation and Verification Techniques

14:00-15:40 | May 11, 2025 @ Sleeping Beauty 1/2

Session Chair: **Xuanqi Chen**, Huawei Design Automation Lab, Hong Kong

14:00-14:20 | Paper ID: 91

Title: AnalogTester: A Large Language Model-Based Framework for Automatic Testbench Generation in Analog Circuit Design

Author(s): Weiyu Chen, Chengjie Liu, Wenhao Huang, Jinyang Lyu, Mingqian Yang, Yuan Du, Li Du, Jun Yang

Presenter: **Weiyu Chen**, National Center of Technology Innovation for EDA

Abstract: Recent advancements have demonstrated the significant potential of large language models (LLMs) in analog circuit design. Nevertheless, testbench construction for analog circuits remains manual, creating a critical bottleneck in achieving fully automated design processes. Particularly when replicating circuit designs from academic papers, manual Testbench construction demands time-intensive implementation and frequent adjustments, which fails to address the dynamic diversity and flexibility requirements for automation. AnalogTester tackles automated analog design challenges through an LLM-powered pipeline: a) domain-knowledge integration, b) paper information extraction, c) simulation scheme synthesis, and d) testbench code generation with Tsinghua Electronic Design (TED). AnalogTester has demonstrated automated Testbench generation capabilities for three fundamental analog circuit types: operational amplifiers (op-amps), bandgap references (BGRs), and low-dropout regulators (LDOs), while maintaining a scalable framework for adaptation to broader circuit topologies. Furthermore, AnalogTester can generate circuit knowledge data and TED code corpus, establishing fundamental training datasets for LLM specialization in analog circuit design automation.

14:20-14:40 | Paper ID: 176

Title: OSTC-FRVF: Order Determination and S-TSVD for Constrained Macromodeling of S Parameter

Author(s): Zhiqiu Liu, Dan Niu, Yuyang Cai, Ao Li, Zhou Jin

Presenter: **Dan Niu**, Southeast University

Abstract: Macromodeling for S parameter, obtained by capturing the frequency response of multiport devices, is a crucial methodology for transient simulations. However, current methods face significant challenges in efficiency, reliability, and accuracy. FRVF will exceed the operational memory when applied to a circuit with 384 ports, and the error with an incorrect order is substantial. Algorithms like AAA and ORA may struggle to satisfy the conjugate properties and stability. To overcome these issues, this paper introduces OSTC-FRVF, a comprehensive solution that achieves acceleration, order correction, and constraint satisfaction. For accuracy, OSTC-FRVF establishes an order determination mechanism (O) to balance the relationship between accuracy and complexity. The improved peak detection method calculates the initial order, and Prony Analysis with a new termination condition adjusts the order promptly. For efficiency, to maximally utilize data redundancy to simplify the computational process, OSTC-FRVF designs a two-pronged acceleration method, S-TSVD. The innovative resonance sampling method (S) and the improved truncated singular value decomposition method (T) collaborate synergistically, which fully exploit the data characteristics to enhance the efficiency in macromodeling. For reliability, the constraints satisfaction method (C) addresses the DC preserve, D-passivity, conjugate properties, and stability to facilitate the success of transient simulations. The validity is thoroughly substantiated on circuits of diverse scales, spanning from 2 to 384 ports. OSTC-FRVF achieves an average speedup ratio of 25.69X and a maximum of 40.29X compared to FRVF. And the relative error is generally below 1%.

14:40-15:00 | Paper ID: 183

Title: BPKSR: A Batch Parallel Krylov Subspace Recycling Method for Efficient Periodic Small-Signal Analysis in RF Circuit Simulation

Author(s): Lingyun Ouyang, Chao Jin, Quan Chen

Presenter: **Lingyun Ouyang**, Harbin Institute of Technology; Southern University of Science and Technology

Abstract: Periodic small-signal analysis in RF circuit simulations poses significant computational challenges, particularly when dealing with a large quantity of frequency points. Although Krylov subspace recycling and parallel computing are effective strategies for accelerating this process, their synergistic combination has remained unexplored. We propose BPKSR, a novel parallel multi-thread subspace recycling method specifically designed for periodic AC (PAC) and noise (PNoise) analysis. Initially, the frequency points are partitioned into multiple batches. For each batch, parallel processing of frequency points is carried out, leveraging the reuse of vectors in shared memory to minimize the number of iterations. Subsequently, a subspace is generated or augmented within each batch and then updated in the shared memory for recycling. Additionally, a frequency points allocation scheme is developed by jointly considering both the similarity between right-hand-side (RHS) vectors and the total number of threads, which aims to optimize parallel computational workloads.

15:00-15:20 | Paper ID: 223

Title: Automated SAR ADC Sizing Using Analytical Equations

Author(s): Zhongyi Li, Zhuofu Tao, Yanze Zhou, Yichen Shi, Zhiping Yu, Ting-Jung Lin, Lei He

Presenter: **Zhongyi Li**, Ningbo Institute of Digital Twin

Abstract: Conventional analog and mixed-signal (AMS) circuit designs heavily rely on manual effort, which is time-consuming and labor-intensive. This paper presents a fully automated design methodology for Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) from performance specifications to complete transistor sizing. To tackle the high- dimensional sizing problem, we propose a dual optimization scheme. The system-level optimization iteratively partitions the overall requirements and analytically maps them to subcircuit design specifications, while local optimization loops determines the subcircuits' design parameters. The dependency graph-based framework serializes the simulations for verification, knowledge-based calculations, and transistor sizing optimization in topological order, which eliminates the need for human intervention. We demonstrate the effectiveness of the proposed methodology through two case studies with varying performance specifications, achieving high SNDR and low power consumption while meeting all the specified design constraints.

15:20-15:40 | Paper ID: 226

Title: SMT-Based Analog Layout Retargeting: Multi-Mode Constraint Extraction and Weighted Optimization

Author(s): Jiwen Huang, Hai Qin

Presenter: **Jiwen Huang**, Xiamen University

Abstract: In integrated circuit design, analog layout retargeting technology plays a key role in achieving design migration, optimizing layouts, and enhancing circuit performance. Existing methods face issues of inefficiency and limited flexibility in constraint extraction and layout optimization, especially in complex circuit designs where they struggle to intelligently differentiate between various types of constraints and balance optimization objectives. To address these challenges, this paper proposes an SMT-based layout migration method, which innovatively introduces multi-mode constraint extraction and distance thresholds to enhance the flexibility and accuracy of constraint extraction. Additionally, a weighted cost function is used to optimize the trade-off between area and interconnection length, providing flexibility to meet different design requirements. Experimental results show that this method significantly improves layout quality and solving efficiency in high-constraint-density scenarios.

TECHNICAL SESSIONS

TS 21. Routing, Interconnect, and Partitioning Innovations

14:00-15:40 | May 11, 2025 @ Sleeping Beauty 3

Session Chair: **Peter Chun**, University of Alberta

14:00-14:20 | Paper ID: 92

Title: MAD-EA: A Multi-Mask Driven Evolutionary Algorithm Framework for Macro Placement Refinement

Author(s): Zhen Wang, Jie Wang, Zhihai Wang, Siyuan Xu, Zijie Geng, Mingxuan Yuan, Jianye Hao

Presenter: **Siyuan Xu**, Noah's Ark Lab, Huawei Technologies

Abstract: Macro placement (MP) is essential in designing very large-scale integrated (VLSI) circuits. However, existing MP approaches face two main challenges: the adaptability to different objectives and the consideration of potential impacts on subsequent workflows. To overcome these challenges, an intuitive approach is to refine the placements generated by existing placers, known as macro placement refinement. This paper introduces a novel multi-mask driven evolutionary algorithm framework, MAD-EA, for intelligent adaptive MP refinement. MAD-EA can be seamlessly integrated as a plugin with any placer to refine initial placements. It incorporates diverse metrics such as dataflow, half-perimeter wire length (HPWL), and regularity, aligning with post-MP workflow metrics to enhance power, performance, and area (PPA). To effectively optimize these diverse objectives simultaneously, MAD-EA employs a multi-mask strategy with the Dataflow Mask, HPWL Mask, and Regularity Mask to optimize dataflow, HPWL, and congestion. Experiments show that MAD-EA improves HPWL by up to 33.00\% and congestion by 22.74\% compared to the state-of-the-art methods.

14:20-14:40 | Paper ID: 102

Title: Adaptive Preconditioning Guided by Divergence Analysis for Enhanced VLSI Global Placement

Author(s): Liwen Jiang, Ruiyu Lyu, Fan Yang, Keren Zhu

Presenter: **Liwen Jiang**, Fudan University

Abstract: Global placement is a critical step in modern VLSI physical design. Traditional electrostatic-based analytical placement algorithms, such as ePlace, employ a two-layer optimization loop: an inner loop using Nesterov's gradient descent, and an outer loop updating the density penalty multiplier to progressively enhance the density penalty. However, these conventional update methods often fail to balance the optimization efforts across different nets, leading to suboptimal solutions. In this paper, we introduce an adaptive preconditioning algorithm that addresses these limitations. Our approach utilizes divergence analysis to identify clusters within the placement region, followed by net preconditioning to adjust the optimization efforts accordingly. This ensures a more balanced distribution of optimization efforts across all nets, leading to improved placement quality. Experimental results on the DAC-2012 benchmarks suite demonstrate that our algorithm achieves a reduction in final placement wirelength compared to DREAMPlace, while obtaining an optimal tradeoff between half-perimeter wirelength (HPWL) and iteration count.

14:40-15:00 | Paper ID: 109

Title: Automatic Parameter Tuning System under Multi-threading Nondeterminism

Author(s): Ziyue Han, Jiajie Xu, Hao Yan

Presenter: **Ziyue Han**, Southeast University

Abstract: With the expansion of design scales, the surge of adjustable parameters for electronic design automation (EDA) tools makes manually tuning parameters become time-consuming and challenging.Recent works employ multi-objective Bayesian optimization (BO) for automatic parameter tuning. However,

non-deterministic design results of EDA tools undermine the effectiveness of BO. The existing forking technique, which can obtain reliable results by conducting design in parallel with identical parameter inputs, requires extracomputational resources and runtime. To address results nondeterminism under multithreading mode, our proposed BO framwork employs an oisyex pected hypervolume improvement (NEHVI) acquisition function to conduct parameter tuning. Experimental results demonstrate that our framework achieves superior optimization results with faster convergence compared to state-of-the-artworks.

15:00-15:20 | Paper ID: 130

Title: Addressing Continuity and Expressivity Limitations in Differentiable Physical Optimization: A Case Study in Gate Sizing

Author(s): Yufan Du, Zizheng Guo, Yang Hsu, Zhili Xiong, Seunggeun Kim, David Z. Pan, Runsheng Wang, Yibo Lin

Presenter: **Yufan Du**, Peking University

Abstract: Differentiable optimization is popular for its efficiency and explainability. However, it faces limitations due to its reliance on continuous formulations and constraints on objective expressivity. To address these challenges, we propose a framework combining differentiable methods with gradient clipping and calibration strategies to ensure efficient and targeted optimization. Gate sizing, a key challenge in chip PPA optimization, exemplifies all the challenges with its discrete nature and objective complexity. Applying our proposed differentiable framework to gate sizing, we outperform top contestants in the 2024 ICCAD CAD gate sizing contest in overall quality scores and runtime, with excellent and balanced performance on all important evaluation metrics.

15:20-15:40 | Paper ID: 187

Title: HDPlacer: A Hierarchy and Dataflow-Aware Macro Placer for Modern SoCs

Author(s): Yilin Li, Wei Fu, Hao Gu, Ziran Zhu

Presenter: **Yilin Li**, Southeast University

Abstract: As modern System-on-Chip (SoC) designs incorporate an increasing number of heterogeneous macros, an effective RTL-aware macro placement method becomes crucial for optimizing design performance. This paper presents HDPlacer, a novel macro placement framework that incorporates design hierarchy and dataflow connectivity to improve placement quality. We first construct a hierarchy tree and introduce a hierarchy-aware clustering method to effectively extract logical information and dataflow dependencies. Then, we employ a dataflow-aware analytical approach to determine the initial placement of clusters and a simulated annealing (SA)-based optimization to assign preferred regions for clusters. Finally, we develop a comprehensive analytical-based global placement with dataflow-aware net weighting and differentiable region guidance formulation, in which nets are systematically classified and assigned adaptive weights to enhance modularity and minimize critical path delays. Experimental results on ICCAD 2015 contest benchmarks demonstrate that HDPlacer achieves superior placement quality compared to the state-of-the-art placers RePlAce and Hier-RTLMP.

TECHNICAL SESSIONS

TS 22. Artificial Intelligence in EDA: Library, Innovation and Applications

14:00-15:40 | May 11, 2025 @ Sleeping Beauty 5

Session Chair: **Xingquan Li**, Peng Cheng Laboratory

14:00-14:20 | Invited Talk

Xingquan Li

Peng Cheng Laboratory

Bio.: Xingquan Li is an Associate Professor at Peng Cheng Laboratory. His research interests include EDA and AI for EDA. His team has developed an open-source infrastructure of EDA and toolchain (iEDA). He has published over 60 papers, and received three First-place Awards from ICCAD@CAD Contest in 2017, 2018, and 2022. In 2020, he received the Application Award of Operations Research from the Operations Research Society of China, and the Best Paper Award from ISEDA 2023.

Title: AiEDA-2.0: An Open-source AI-Aided Design (AAD) Library for Design-to-Vector

Abstract: Although artificial intelligence (AI) has made significant progress in the electronic design automation (EDA) field, specialized infrastructure remains insufficient. In this paper, we analyze the necessary components for the integration of AI with EDA, propose a data decomposition from design to vector, and build an open-source AI-aided design (AAD) library. This library aims to transform chip data into vectors, train AI4EDA models, and integrate trained models into the chip design flow.

14:20-14:40 | Paper ID: 9

Title: PZ-Agent: A Symbolic-Engine Enhanced LLM Agent for Op-Amp Topology Inquisition

Author(s): Mingzhen Li, Bo Li, Tingjie Yang, Guoyong Shi

Presenter: **Mingzhen Li**, Shanghai Jiao Tong University

Abstract: Using large language models (LLMs) for EDA is a rising research interest. In this paper, we investigate whether a symbolic tool assisted LLM agent is capable of offering circuit level inference in the analog domain. We develop a framework to inject pole-zero (PZ) knowledge into a LLM-based multi-agent system, hoping that this PZ-agent so formed can handle Op-amp topology inquisition. We demonstrate in details that analytical knowledge in the PZ form should be properly condensed to better the reasoning capability of the PZ-agent. It turns out that, with proper incorporated knowledge, the PZ-agent is capable of answering designer's inquiries on certain sophisticated multi stage Op-amp design issues.

14:40-15:00 | Paper ID: 35

Title: SpecLLM: Exploring Generation and Review of VLSI Design Specification with Large Language Model

Author(s): Mengming Li, Wenji Fang, Qijun Zhang, Zhiyao Xie

Presenter: **Mengming Li**, The Hong Kong University of Science and Technology

Abstract: The development of architecture specifications is an initial and fundamental stage of the integrated circuit (IC) design process. Traditionally, architecture specifications are crafted by experienced chip architects, a process that is not only time-consuming but also error-prone. Mistakes in these specifications may significantly affect subsequent stages of chip design. Despite the presence of advanced electronic design automation (EDA) tools, effective solutions to these specification-related challenges remain scarce. Since writing architecture specifications is naturally a natural language processing (NLP) task, this paper pioneers the automation of architecture specification development with the advanced capabilities of large language models (LLMs).

We propose a structured definition of architecture specifications, categorizing them into three distinct abstraction levels. Based on this definition, we create and release a specification dataset by methodically gathering 46 architecture specification documents from various public sources. Leveraging our definition and dataset, we explore the application of LLMs in two key aspects of architecture specification development: (1) Generating architecture specifications, which includes both writing specifications from scratch and converting RTL code into detailed specifications. (2) Reviewing existing architecture specifications. We got promising results indicating that LLMs may revolutionize how these critical specification documents are developed in IC design nowadays.

15:00-15:20 | Paper ID: 43

Title: DiffuSE: Cross-Layer Design Space Exploration of DNN Accelerator via Diffusion-Driven Optimization

Author(s): Yi Ren, Chenhao Xue, Jiaxing Zhang, Chen Zhang, Qiang Xu, Yibo Lin, Lining Zhang, Guangyu Sun

Presenter: **Yi Ren**, Peking University

Abstract: The proliferation of deep learning accelerators calls for efficient and cost-effective hardware design solutions, where parameterized modular hardware generator and electronic design automation (EDA) tools play crucial roles in improving productivity and final Quality-of-Results (QoR). To strike a good balance across multiple QoR of interest (e.g., performance, power, and area), the designers need to navigate a vast design space, encompassing tunable parameters for both hardware generator and EDA synthesis tools. However, the significant time for EDA tool invocations and complex interplay among numerous design parameters make this task extremely challenging, even for experienced designers. To address these challenges, we introduce DiffuSE, a diffusion-driven design space exploration framework for cross-layer optimization of DNN accelerators. DiffuSE leverages conditional diffusion models to capture the inverse, one-to-many mapping from QoR objectives to parameter combinations, allowing for targeted exploration within promising regions of the design space. By carefully selecting the conditioning QoR values, the framework facilitates an effective trade-off among multiple QoR metrics in a sample-efficient manner. Experimental results under 7nm technology demonstrate the superiority of the proposed framework compared to previous arts.

15:20-15:40 | Paper ID: 63

Title: Unsupervised Defect Detection Based on Self-Supervised Transformers

Author(s): Qianqian Ye, Hui Jiang

Presenter: **Qianqian Ye**, Semitronix Corporation

Abstract: Effective management of wafer defects is crucial for improving the yield of integrated circuit (IC) chip manufacturing. Compared to traditional defect analysis performed by human experts, deep learning-based automatic defect detection can significantly enhance both the speed and accuracy of the process. This helps engineers identify root causes more quickly, thereby improving yield. However, the training of these detection models requires substantial manual annotation, which can be costly and limits the widespread application of automatic defect detection. To address this challenge, we propose an unsupervised defect localization method that requires no training data. This method achieved a defect detection accuracy (ACC) of 92.5% (with IoU threshold = 0.3) on both scanning electron microscopy (SEM) and optical microscope (OM) images. By significantly reducing the need for manual annotation, this new approach paves the way for fully automated large-scale data training in the future.

TECHNICAL SESSIONS

TS 23. Advanced Timing Analysis and Optimization

10:40-12:00 | May 12, 2025 @ Sleeping Beauty 1/2

Session Chair: Yibo Lin, Peking University

10:40-11:00 | Paper ID: 59

Title: A Statistical Static Timing Analysis Algorithm Based On Graph Neural Network

Author(s): Yufan Chen, Leyun Tian, Yuyang Ye, Chenpu Shi, Hao Yan

Presenter: **Yufan Chen**, Southeast University

Abstract: Satistical static timing analysis (SSTA) struggles with nonlinear MAX operations, which is crucial in block based statistical timing analysis. Most existing methods either incur high computational costs or rely on inaccurate approximations. In this work, we propose a SSTA algorithm based on graph neural network (GNN) to deal with non-Gaussian while balancing speed by using its node regression function. GNN eliminate the traversal propagation through message passing mechanisms and can simulate the nonlinear behavior of MAX operation through its attention mechanisms. Experimental results demonstrate that our model outperforms the First-order delay model and Skew-normal delay model in terms of accuracy, especially when skewness has a significant impact, while its time overhead is on the same order of magnitude as First-order model. Taking into account both accuracy and runtime, our proposed model has significant computational efficiency advantages while ensuring high prediction accuracy.

11:00-11:20 | Paper ID: 81

Title: Pre-Routing Timing Estimation Considering Power Delivery Network

Author(s): Mingwei He, Leyun Tian, Yaning Jia, Yuyang Ye

Presenter: **Mingwei He**, Southeast University

Abstract: In recent years, the demand for fast and accurate pre-routing timing prediction is increasing. However, existing machine learning (ML)-based methods for predicting pre-routing timing often overlook the impact of power delivery networks (PDNs), which are critical to IR drop and routing congestion, limiting the effectiveness of these approaches in real-world circuit designs. To address this challenge, we propose a multi-modal model that integrates PDN, layout, and netlist data. Additionally, we incorporate auxiliary and contrastive learning techniques to capture the differences across various PDNs. Extensive experiments on open-source designs demonstrate the superior performance of our model.

11:20-11:40 | Paper ID: 179

Title: Fast and Effective Logic Gate Sizing Based on Heterogeneous Graph Neural Network

Author(s): Yuhan Dong, Junming Jiao, Han Zhang, Yusen Qin, Zeyuan Deng, Xu Cheng, Peng Cao

Presenter: **Yuhan Dong**, Southeast University

Abstract: Gate sizing serves as a fundamental netlist optimization technique for enhancing performance and power in the physical design flow. Traditional heuristic sizing algorithms prove computationally expensive, while existing machine learning approaches do not fully capture the influence of neighboring instances. In this work, we present a fast and effective end-to-end algorithm for post-placement logic gate sizing. It combines recursive feature elimination, a heterogeneous graph neural network encoder, and function-specific prediction heads to capture multiscale graph information and learn high-quality instance representations, delivering accurate sizing solutions. Experimental results on ICCAD 2024 Contest benchmarks demonstrate that our method eliminates 98.6% of negative slacks, along with 99.2% of slew and load violations, achieving 12.86x

acceleration over median contestant runtime. In terms of the contest evaluation metric, which balances performance gains, power savings, and computational efficiency, our approach secured third place in the contest.

11:40-12:00 | Paper ID: 42

Title: A Configurable Piecewise-Linear Approximation Squarer with Unbiased Error Compensation for Energy-Efficient Floating-Point Computing

Author(s): Wenjing Huang, Yingde Li, Chenyi Wen, Haonan Du, Cheng Zhuo

Presenter: **Wenjing Huang**, Zhejiang University

Abstract: Approximate computing has emerged as a promising paradigm to enhance energy efficiency in applications where strict computational accuracy is not essential. In this work, we propose PAS, a piecewise-linear approximate floating-point squarer with unbiased error compensation and runtime configurability. PAS employs linear interpolation to iteratively approximate the square function, achieving configurability through multi-level error compensation. To optimize per formance, we design a multi-level, parallelizable circuit architecture that relies solely on negation and shifting operations, significantly reducing hardware complexity. Additionally, we introduce a runtime-configurable tree structure that dynamically adapts to varying precision requirements, making PAS highly versatile for diverse application scenarios. Compared to state-of-the-art approximate squarers and multipliers, PAS achieves a superior balance between accuracy and resource efficiency. Experimental results demonstrate that PAS significantly reduces errors, with improvements of over 30% in MAE and 53% in MSE compared to existing designs, while also reducing area-delay product (ADP) by 13-42%. Application-level evaluations, such as in square-law demodulation (SLD), further validate PAS's effectiveness, showing that it achieves the best signal-to-noise ratio (SNR) and Euclidean distance performance, even when compared to exact squarers. These results highlight PAS as a highly efficient and adaptable solution for energy-constrained applications requiring approximate squaring operations.

TECHNICAL SESSIONS

TS 24. System-Level Design Exploration and NoC Innovations

10:40-12:00 | May 12, 2025 @ Sleeping Beauty 3

Session Chair: Jianan Mu, Institute of Computing Technology, Chinese Academy of Sciences

10:40-11:00 | Paper ID: 66

Title: CIR-NoC: Accelerating CNN Inference Through In-Router Computation During Network Congestion

Author(s): Cuiyu Qi, Yi Liu, Hui Chen, Fen Ge, Weiqiang Liu

Presenter: **Cuiyu Qi**, Nanjing University of Aeronautics and Astronautics

Abstract: Traditional Network-on-Chip (NoC) architectures frequently suffer from network congestion when processing complex Convolutional Neural Network (CNN) models, primarily due to the massive data volume and computation-intensive tasks. To address this issue, this paper proposes a new NoC-based CNN acceleration architecture. The core innovation involves integrating computational units into routers, thereby exploiting network congestion periods for in-router computations and alleviating the impact of NoC congestion on CNN inference efficiency. Focusing on activation operations as a representative case, we conduct experiments with three CNN models: LeNet, AlexNet, and ResNet. Experimental results demonstrate that, compared to the conventional VC-based router baseline, the proposed architecture achieves inference cycle reductions of 5.72%–6.64%, 5.12%–5.53%, and 4.53%–5.30% for the three models under varying NoC configurations (4×4, 8×8, and 16×16 mesh topologies). These results validate that the proposed architecture significantly improves inference efficiency. Additionally, we design two optimization strategies based on the architecture and provide a systematic analysis of their effectiveness and applicability across different CNN models.

11:00-11:20 | Paper ID: 68

Title: MULiN: A NoC-DNN Accelerator Based on In-Network Multiplication

Author(s): Yi Liu, Cuiyu Qi, Hui Chen, Kai Chen, Yuxiang Fu, Li Li

Presenter: **Yi Liu**, Nanjing University

Abstract: The rapid advancement of deep learning has driven the remarkable success of Deep Neural Networks (DNNs) across various domains. However, the computational and data transmission complexity of DNN models presents significant challenges to traditional hardware architectures. Network-on-Chip (NoC)-based DNN accelerators have emerged as a promising solution to address these challenges. To improve DNN inference speed and alleviate the impact of network congestion on computational efficiency, this paper presents a NoC architecture with in-network multiplication. By embedding multiplication units within the NoC routers, partial computations are offloaded during periods of network congestion, thereby enhancing overall system efficiency. We develop a cycle-accurate NoC-DNN simulator. Under NoC scales of 8×8 and 16×16, the inference speeds of LeNet and AlexNet-like models are improved 10.7%, 6.9%, 16.3%, and 15.5%, respectively.

11:20-11:40 | Paper ID: 168

Title: VeriRAG: Design AI-Specific CPU Co-processor with RAG-Enhanced LLMs

Author(s): Kangbo Bai, Peiran Yan, Lifeng Liu, Tianyu Jia

Presenter: **Kangbo Bai**, Peking University

Abstract: In recent years, many industrial CPUs have integrated AI-specific co-processors as "CPU for AI" solution. However, the implementation details of co-processors are diverse. In this work, we present VeriRAG, an LLM-assisted agile design methodology for AI-specific CPU co-processor, which includes a

summary-template RAG-enhanced LLM flow for agile RTL generation. We first present a general RISC-V-based AI-specific co-processor architecture template to support both Matrix and Nonlinear computations with detailed instruction extensions. Furthermore, we develop a series of AI-specific co-processors based on VeriRAG for different CPUs, i.e., high-end Xuantie C910 and low-power CVA6 CPU. It is observed that the AI co-processors can be effectively and properly designed by VeriRAG within a short design cycle, and co-processors gain notable performance boost for AI tasks.

11:40-12:00 | Paper ID: 171

Title: ArchBot: A Labour-free Processor Architecture Design Framework via Experienced LLM

Author(s): Zheng Wu, Zhuoyuan Yang, Zihao Chen, Changxu Liu, Fan Yang

Presenter: **Zheng Wu**, Fudan University

Abstract: Processors are the cornerstone of computing systems, yet their design process remains highly complex and labor-intensive. Current automated architecture design methods often rely on pre-configured models, limiting flexibility and requiring extensive manual effort. Additionally, challenges such as capturing architectural knowledge, optimizing parameters within constrained simulation times, and managing complex decision-making processes further complicate the task. To address these issues, we propose ArchBot, a labor-free processor architecture design framework leveraging large language models and reinforcement learning. ArchBot integrates a curated RISC-V architecture knowledge base, RL for microarchitecture exploration, and a machine-learning-based fast simulation model to accelerate optimization. It also uses LLMs to automate design requirement analysis and task decomposition, generating the gem5 code as output. Experiments demonstrate that ArchBot achieves a 95% success rate in meeting design requirements, surpassing existing frameworks and offering a novel solution for automated processor design.

TECHNICAL SESSIONS

TS 25. RTL and Gate-Level Simulation and Verification

10:40-12:00 | May 12, 2025 @ Snow White 2/3

Session Chair: **Hongce Zhang**, The Hong Kong University of Science and Technology (Guangzhou)

10:40-11:00 | Paper ID: 51

Title: Extend IVerilog to Support Batch RTL Fault Simulation

Author(s): Jiaping Tang, Jianan Mu, Zizhen Liu, Zhiteng Chao, Jing Ye, Huawei Li

Presenter: **Jianan Mu**, Institute of Computing Technology, Chinese Academy of Sciences

Abstract: The advancement of functional safety has made RTL-level fault simulation increasingly important to achieve iterative efficiency in the early stages of design and to ensure compliance with functional safety standards. In this paper, we extend IVerilog to support batch RTL fault simulation and integrate the event-driven algorithm and the concurrent fault simulation algorithm. Comparative experiments with a state-of-the-art commercial simulator and an open-source RTL fault simulator demonstrate that our simulator achieves a performance improvement of 2.2× and 3.4×, respectively.

11:00-11:20 | Paper ID: 142

Title: Auto-CEC: Combinational Equivalence Checking via Intelligent Sweeping Engine Selection

Author(s): Haonan Wei, Wentao Jiang, Zhang Hu, Zhengyuan Shi, Yinshui Xia, Lunyao Wang, Zhufei Chu

Presenter: **Haonan Wei**, Ningbo University

Abstract: Combinational Equivalence Checking (CEC) is essential for circuit verification, but traditional heuristic-based sweeping engine selection often results in inefficiencies. To address this, we enhance the previous Hybrid-CEC method by integrating proposed BDD sweeping, which significantly improves performance for circuits with high XOR chain density, achieving a 13.27× speed-up over Kissat solver. To address the lack of effective guidance for solvers in different verification scenarios, we propose the Auto-CEC framework. This intelligent framework leverages DeepGate2 embeddings and a convolutional neural network (CNN)-based classifier to dynamically predict the mostsuitable sweeping engine. Experimental results on industrial benchmarks demonstrate that Auto-CEC effectively balances accuracy and efficiency, achieving speed-ups of 6.02× to 11.29×over existing approaches.

11:20-11:40 | Paper ID: 170

Title: OSCC-SA: Detecting Oscillation in Strongly Connected Components Using Static Analysis

Author(s): Han Zhang, Xu Cheng, Junming Jiao, Yusen Qin, Peng Cao

Presenter: **Han Zhang**, Southeast University

Abstract: Combinational logic loops present critical design challenges by inducing signal contention and sustained oscillations, leading to excessive power dissipation and functional anomalies in integrated circuits. Prior methods have primarily focused on full condition generation for potential oscillations. However, these methods come with exponential complexity (O(2^n)) and often overlook the efficiency that can be gained by directly detecting oscillations, causing inefficient resource utilization. In this work, we propose OSCC-SA, an open-source static analysis framework directly detecting oscillatory behaviour in Strongly Connected Components (SCCs), the fundamental topological manifestation of combinational loops. We develop an enhanced SCC benchmark generation methodology building upon the 2024 Integrated Circuit EDA Elite Challenge dataset, incorporating comprehensive complexity metrics. Our experimental results demonstrate that the proposed loop-based reverse search algorithm achieves linear-time complexity (O(n)) across all

benchmarks while maintaining 100% detection accuracy. The practical efficacy of OSCC-SA has been recognized with the first-class award at the Challenge.

11:40-12:00 | Paper ID: 212

Title: A Two-Stage Optimization Framework for Logic Replication in Hypergraph Partitioning

Author(s): Qiwang Chen, Shunyang Bi, Hailong You, Zehong Wei, Kexin Zhang, Jing Tang

Presenter: **Qiwang Chen**, Xidian University

Abstract: With the explosive growth in the complexity of integrated circuit designs, hardware emulation platforms face significant challenges in simulating designs with billions of gates using a single Field-programmable Gate Array (FPGA). This paper proposes a two-phase optimization framework: first, an initial hypergraph partitioning is performed using an improved FM algorithm, followed by the application of a targeted logic replication strategyv that consider the cost-effectiveness of replication on the partitioned results. By adopting the two-stage optimization strategy, our method maintains algorithmic efficiency while reducing computational complexity. Experimental results demonstrate that, compared to non-replication strategies, our approach achieves an average reduction of 17% in total hop distance while completing logic replication in a significantly shorter time, validating the effectiveness of phased optimization strategy.

TECHNICAL SESSIONS

TS 26. Packaging, Chiplet Design, and Multi-Physics Simulation

10:40-12:00 | May 12, 2025 @ Snow White 1

Session Chair: **Changkai Yu**, Jaguar Micro

10:40-11:00 | Paper ID: 21

Title: Hierarchical Decomposition and Interconnection Method for Efficient Thermal Simulation of Chiplet-Based 2.5D Systems

Author(s): Shunxiang Lan, Min Tang, Junfa Mao

Presenter: **Shunxiang Lan**, Shanghai Jiao Tong University

Abstract: Thermal simulation is a key step in validating the performance of chiplet-based 2.5D systems. However, when dealing with the temperature-dependent parameters, the global nonlinear iteration may result in heavy computational cost. In this paper, an efficient hierarchical decomposition and interconnection (HDI) method is proposed for efficient thermal simulation of chiplet-based 2.5D systems. Firstly, the HDI method resolves the 2.5D system into two parts: the linear region and the nonlinear region. In the transient simulation, the response of the linear region is divided into a zero-input (ZI) one and a zero-state (ZS) one. In order to characterize the linear time-invariant properties of the ZS response, the impact of the linear region is further decomposed into the contributions of the face elements at the interface. In this way, an equivalent thermal boundary condition in the form of the thermal resistance matrix is established to represent the linear region. Then, we combine it with the nonlinear region to calculate the complete response in the interconnection process. By this means, the tedious iteration is confined to the nonlinear region, thereby reducing the computational complexity and improving the efficiency. To validate the accuracy and efficiency of the proposed HDI method, thermal simulation of a typical chiplet-based 2.5D system is performed, and a speed-up of 48× is achieved compared to the conventional finite volume method.

11:00-11:20 | Paper ID: 55

Title: Transformer-based S-parameter Extraction for Coupled Transmission Lines with Vias

Author(s): Qin Li, Yanliang Sha, Hao Zhou, Quan Chen

Presenter: **Qin Li**, Southern University of Science and Technology

Abstract: S-parameters are a crucial tool for simulating and analyzing high-speed, high-frequency signal transmission, particularly in advanced packaging and PCB designs such as chiplets and 3DICs. However, traditional 2.5D/3D electromagnetic (EM) field solvers are computationally expensive and time-intensive, making them impractical for agile and automated design iterations. Existing neural network-based methods for S-parameter prediction are often limited to predefined 2D planar structures, restricting their applicability. In this work, we propose SFormer, a transformer-based deep learning framework that predicts the S-parameters of coupled transmission line pairs directly from their layout while supporting highly flexible configurations. Our method accounts for variations in multiple layout parameters, including line length, segmentation, bending direction, line spacing, line width, and line-to-ground distance. The layout is represented as a graph, processed by a graph convolutional network (GCN) to extract geometric and topological features, which are then refined by a transformer encoder. Finally, a multi-layer perceptron (MLP) predicts the corresponding S-parameter matrix elements. Additionally, we introduce a specialized scheme for efficiently generating S-parameters of multi-layer transmission lines connected by vias, enabling rapid extraction for truly 3D structures. Compared to commercial EM solvers, SFormer achieves over 500× speed improvement while maintaining a mean absolute error (MAE) below 1e-2 for 4-port network extraction up to 15 GHz in commercial design cases.

11:20-11:40 | Paper ID: 96

Title: Graph Sequence-Based Prediction of Electrothermal Stress Evolution for Power Delivery Networks

Author(s): Yuwei Sun, Yunfan Zuo, Jiajun Shen, Pinquan Li, Hao Yan, Longxing Shi

Presenter: **Yuwei Sun**, Southeast University

Abstract: With the advancement of integrated circuit technology, electrothermal migration (EM-TM) in power delivery networks (PDNs) has become a key reliability challenge. Existing machine learning methods predict hydrostatic stress distributions in interconnects by avoiding computationally intensive Korhonen equation solutions. At the same time, they are unable to capture the trajectory of evolution of stress and actively seek the exact moment of failure occurrence. We propose a spatiotemporal graph-based prediction framework that integrates spatial structural features and captures early stress accumulation patterns from input sequences, enabling long-term forecasting of EM-TM coupling evolution. The experimental results show that our approach achieves higher prediction accuracy and stability on PDN datasets spanning up to 1,500 interconnect segments. Furthermore, it achieves a near 5× speedup in prediction compared to the single-timestep SOTA model and a 6896× acceleration over the commercial software COMSOL.

11:40-12:00 | Paper ID: 126

Title: ATSim3.5D: A Multiscale Thermal Simulator for 3.5D-IC Systems based on Nonlinear Multigrid Method

Author(s): Qipan Wang, Tianxiang Zhu, Yibo Lin, Runsheng Wang, Ru Huang

Presenter: **Qipan Wang**, Peking University

Abstract: To resolve the rising temperatures in 3.5D-ICs, a thermal-aware design flow becomes increasingly crucial, necessitating an ac- curate and efficient thermal simulation tool. However, previous tools struggle to handle the unique heterogeneous multiscale structures in 3.5D-ICs and the nonlinear thermal effects caused by high temperatures. In this work, we present a multiscale thermal simulator for 3.5D-ICs. We propose a hybrid tree structure to generate multilevel grids and capture the multiscale features and employ the nonlinear multigrid method for quick solving. Compared to ANSYS Icepak, it exhibits high accuracy (mean absolute relative error < 1%, max error < 2 ℃), and efficiency (80× acceleration), delivering a powerful means to evaluate and refine thermal designs.

TECHNICAL SESSIONS

TS 27. Advanced Simulation and Optimization in Semiconductor Processes

10:40-12:00 | May 12, 2025 @ Sleeping Beauty 5

Session Chair: **Lang Zeng**, Beihang University

10:40-11:00 | Paper ID: 175

Title: A Scalable Machine Learning based Device Model with Mixture-of-Expert Neural Networks for Enhanced Accuracy and Efficiency

Author(s): Yuxiang Zhou, Baokang Peng, Zian Wang, Yu Li, Runsheng Wang, Lining Zhang

Presenter: **Yuxiang Zhou**, Peking University

Abstract: This paper proposes a novel global modeling framework based on a Mixture of Experts (MoE) architecture to address the challenge that conventional compact global models face in capturing the size-dependent operational characteristics of gate-all-around field-effect transistor (GAAFET). The proposed framework dynamically activates specialized expert models through an adaptive gating network, effectively integrating device geometric parameters with bias voltage conditions to enable precise prediction of device current characteristics. Comprehensive experimental results demonstrate that the proposed MoE-based model can significantly improve prediction accuracy while ensuring computational efficiency, especially when dealing with high-dimensional and complex current voltage (IV) characteristics, exhibiting strong adaptability and generalization ability. Compared to conventional global models with equivalent parameter counts, the proposed method reduces root mean square error (RMSE) by 20.97% while accelerating inference speed by 53.57%. When benchmarked against models with comparable inference speeds, it achieves superior performance with 54.26% lower RMSE and 48.88% reduced mean absolute percentage error (MAPE). These results highlight the framework's strong adaptability to device scaling variations and enhanced generalization capabilities across diverse operating regimes.

11:00-11:20 | Paper ID: 196

Title: Wide-Band ANN-based Modeling of Inductors for 0.1um GaAs pHEMT Process

Author(s): Linxin Chen, Xiaotian Song

Presenter: **Linxin Chen**, Zhejiang University

Abstract: A wide-band ANN-based inductor model up to 110GHz for 0.1um GaAs pHEMT technology is presented. Different with the traditional equivalent circuit structure, the proposed ANN model takes high-order parasitic effect into account, such as skin effect and coupling effect, which is significant in high-frequency applications. The proposed ANN model has the input layer of geometric dimensions of the inductor and the frequency, with S-parameters as the output layer. The relationship between inputs and outputs is described through nonlinear expressions training of the model. The model results demonstrate high accuracy in comparison with the EM simulation results across the 110GHz frequency range. By integrating into the PDK, the efficiency and accuracy of MMIC design can be significantly enhanced.

11:20-11:40 | Paper ID: 210

Title: Towards Accurate Machine-learning-assisted Aging Prediction with Probabilistic Strategy

Author(s): Xiaoxiao Qiu, Daoda An, Yixian Wang, Pengpeng Ren, Zhigang Ji

Presenter: **Xiaoxiao Qiu**, Shanghai Jiao Tong University

Abstract: Aging delay prediction is one of the key tasks for modern circuit design during reliability assessment. In traditional methods, static timing analysis is utilized to estimate accurate and effective guard bands.

However, it requires intensive Monte-Carlo simulations which could bring high computational overheads. In modern IC design, deployment of neural networks assists to shorten time consumption and enhance prediction efficiency. Due to the black-box training procedure, the prediction results usually suffer from the uncertainty in networks and prediction accuracy could be unsatisfying in some risk-sensitive applications. In this work, we proposed a simple method to improve the aging delay predicted by machine-learning-based method. By implementing uncertainty estimates based on hybrid graphic neural distribution with Monte Carlo network and Dropout, prediction accuracy can be enhanced without further training while enabling the network to maintain high efficiency. Then, statistical analysis is developed based on predictive distribution and an innovative scheme for guard bands design is provided. Experiment results demonstrate that our method shows higher accuracy compared with benchmark networks with uncertainty unconsidered.

11:40-12:00 | Paper ID: 211

Title: Recurrent Neural Network Based Aging Open Model Interface for AI-based Compact Model

Author(s): Shuhan Wang, Zheng Zhou, Yongjia Wang, Xiaoyan Liu, Xing Zhang

Presenter: **Shuhan Wang**, Peking University

Abstract: In this work, a Recurrent Neural Network-based Open Model Interface (RNN-OMI) is proposed to enable AI driven compact model (CM) to characterize the typical aging behavior of MOSFETs, specifically Negative Bias Temperature Instability (NBTI). The long-term sequence learning ability of RNN assists in fine-tuning the sensitive parameters within AI-CM. The enhanced AI-CM predicts the drift of SRAM butterfly curves, enabling the temporal prediction in circuit aging evaluation.

POSTER SESSION

15:40-16:00 | May 10, 2025 | Poster Area of Conference Center @ Disneyland Hotel

Poster No.: P01
Paper ID: 12
Paper Title: ULBNN: Ultra-lightweight BNN Accelerator for Out-Of-Order Execution in Autonomous Driving
Author(s): Mingke Xiao, Guanglong Qu, Yutong Jia, Linlin Xiao, Yukuan Chang, Yue Su, Xu Zhang
Presenter: **Mingke Xiao**, Hangzhou Institute for Advanced Study, University of Chinese Academy of Sciences

Poster No.: P02
Paper ID: 16
Paper Title: A Computing-in-Memory Proposal for STT-MRAM Based on PhaseFET Device Detection
Author(s): Yongliang Zhou, Yufei He, Jingxue Zhong, Yingxue Sun, Chunyu Peng, Xiulong Wu
Presenter: **Yufei He**, Anhui University

Poster No.: P03
Paper ID: 41
Paper Title: An Analytical Global Placement Algorithm With A New Self-Adaptive Wirelength Model
Author(s): Weijie Chen, Taihua Liang, Bin Liao
Presenter: **Weijie Chen**, Shenzhen University

Poster No.: P04
Paper ID: 45
Paper Title: Study on Reduced Order Thermal Models for 3D Electronics Cooling Simulation with Variable HTCs
Author(s): Zhizhu Cao, Jiming Li
Presenter: **Zhizhu Cao**, Huawei Company

Poster No.: P05
Paper ID: 53
Paper Title: A Post-Layout Driven Analog Circuit Automatic Sizing Framework Verified With A Rail-to-Rail Operational Amplifier
Author(s): Heng Zhang, Xin Lu, Mingqian Yang, Yize Wang, Yuan Du, Li Du
Presenter: **Heng Zhang**, Nanjing University

Poster No.: P06
Paper ID: 54
Paper Title: Co-Placement of I/O Pins and Cells with Multi-Electrostatics Modeling
Author(s): Kexin Zhao, Fuxing Huang, Wenxing Zhu
Presenter: **Kexin Zhao**, Fuzhou University

Poster No.: P07
Paper ID: 72
Paper Title: An Analytical Electrical-Thermal Coupling Model for TSV with Non-Uniform Substrate Temperature
Author(s): Xiaoning Ma, Qinzhi Xu, Zeyu Sun, Chenghan Wang, Hao He, Kunlong An, Jianyun Liu, He Cao, Daoqing Zhang, Tunan Sun, Zhiqiang Li
Presenter: **Qinzhi Xu**, Institute of Microelectronics of the Chinese Academy of Sciences

Poster No.: P08
Paper ID: 76

Paper Title: Thermal Modeling and Improvement of 2.5D Chiplet-based Heterogeneous System with Thermal Through Silicon Via
Author(s): Wen Shi, Yijiao Wang, Jiayao Wu, Tao Zou, Ruotong Liu, Hui Zhang, Fei Liu, Weisheng Zhao
Presenter: **Wen Shi**, Beihang University

Poster No.: P09
Paper ID: 78
Paper Title: AutoRRAM: An Agile RRAM Compiler Featuring Simultaneous Layout/Netlist Generation and Cross-Technology Migration
Author(s): Tianze Wu, Zezhi Chen, Chenkai Chai, Jinglei Hao, Qian Qin, Yukai Lu, Zhichao Lu, Zuochang Ye, Liang Zhao
Presenter: **Tianze Wu**, Zhejiang University

Poster No.: P10
Paper ID: 87
Paper Title: ApproxPilot: A GNN-based Accelerator Approximation Framework
Author(s): Qing Zhang, Siting Liu, Yajuan Hui, Cheng Liu
Presenter: **Cheng Liu**, Institute of Computing Technology, Chinese Academy of Sciences

Poster No.: P11
Paper ID: 94
Paper Title: An Agile Design Method for Reconfigurable Spatial Accelerators in Tensor Computation
Author(s): Zhipeng Wu, Yu Liu, Ning Li, Heng Cao, Han Wang
Presenter: **Ning Li**, Tianjin University

Poster No.: P12
Paper ID: 104
Paper Title: A ReRAM-Based Adaptive Binary Neural Network Accelerator for Efficient Inference
Author(s): Peng Dang, Bin Huang, Huawei Li
Presenter: **Peng Dang**, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences

Poster No.: P13
Paper ID: 111
Paper Title: RAPlace: Macro Placement with Reinforcement Learning
Author(s): Hu Liu, Yujie Lin, Yue Wu, Xiaoyan Yang
Presenter: **Hu Liu**, Hangzhou Dianzi University

Poster No.: P14
Paper ID: 144
Paper Title: STPSim: Accelerating Circuit Simulation via Semi-Tensor Product-Based Parallelism
Author(s): Chengkai Qiu, Yanzhen Wang, Hongyang Pan, Yinshui Xia, Lunyao Wang, Zhufei Chu
Presenter: **Chengkai Qiu**, Ningbo University

Poster No.: P15
Paper ID: 149
Paper Title: GAS: A Flexible CNN Accelerator Architecture for Heterogeneous Dataflow Implementation
Author(s): Jiaxin Zhang, Ning Li, Zhipeng Wu, Yu Liu
Presenter: **Ning Li**, Tianjin University

Poster No.: P16
Paper ID: 153

Paper Title: Modeling of Small Source/Drain Defect in FinFET for Cell-Aware Test
Author(s): Jianghao Ma, Wangjun Yang, Mingyu Ma, Shujun Gao, Jiaxing Gao, Siqi Duan, Hailong You, Cong Li
Presenter: **Jianghao Ma**, Xidian University

Poster No.: P17
Paper ID: 158
Paper Title: DSEAcc: A Fast and Flexible Design Space Exploration Framework for Approximate Accumulators
Author(s): Liping Wang, Xianghui Fu, Lingjun Xi, Yike Wang, Yu Gong
Presenter: **Liping Wang**, Nanjing University of Aeronautics and Astronautics

Poster No.: P18
Paper ID: 160
Paper Title: Computing Quality Driven Agile Design Space Exploration for Approximation based Matrix-Vector-Multiplication
Author(s): Lingjun Xi, Liping Wang, Xianghui Fu, Yaofu Sun, Chaojie Wei, Yu Gong
Presenter: **Lingjun Xi**, Nanjing University of Aeronautics and Astronautics

Poster No.: P19
Paper ID: 167
Paper Title: Interleave Lock: An SAT Attack Resistant Logic Lock for Logic Circuits
Author(s): Yang Zeng, Xiaole Cui, Juncheng Pu
Presenter: **Yang Zeng**, Peking University Shenzhen Graduate School

Poster No.: P20
Paper ID: 169
Paper Title: An Automated Method for Eliminating Oscillation in Combinational Logic Circuit
Author(s): Boyu Shi, Yilong Li, Wanying Yuan, Qingsheng Qiu, Ziwen Zheng, Chao Wang
Presenter: **Boyu Shi**, Southeast University

Poster No.: P21
Paper ID: 181
Paper Title: A Satisfiability Based Method to Analyze Combinationality of Cyclic Circuits
Author(s): Jingru Lyu, Hailong You
Presenter: **Jingru Lyu**, Xidian University

Poster No.: P22
Paper ID: 191
Paper Title: Stackable Thermal Model for 3D Integration
Author(s): Xiangqiao Meng, Yiming Zhang, Yuzhi Liu, Ping Li, Chen Wu, Lei He
Presenter: **Xiangqiao Meng**, Eastern Institute for Advanced Study, Eastern Institute of Technology; The Hong Kong Polytechnic University

Poster No.: P23
Paper ID: 199
Paper Title: CAPlace: A College Admission Parallel Detailed Placement Method for FPGAs
Author(s): Zheng Wang, Minghua Shen
Presenter: **Zheng Wang**, Sun Yat-sen University

Poster No.: P24
Paper ID: 204
Paper Title: Hybrid Automation in Analog Sizing: Synergizing Designer Intuition with Multi-Objective Optimization for Gain-Boosted Amplifiers

Author(s): Yue Huang, Wangzhen Li, Xiaochuan Peng, Keren Zhu, Fan Yang, Xuan Zeng
Presenter: **Yue Huang**, Fudan University

Poster No.: P25
Paper ID: 208
Paper Title: Simulating CXL Shared Coherent Memory Using Shared Memory Among Virtual Machines
Author(s): Ting Wu, Linbo Long, Zhulin Ma, Qiushuang Yu, Hang Tian, Weichen Liu
Presenter: **Ting Wu**, Chongqing University of Posts and Telecommunications

Poster No.: P26
Paper ID: 215
Paper Title: A Novel VLSI Clock Tree Synthesis Method Based on Manhattan Ring Clustering
Author(s): Zhenghua Zhou, Zexi Xie, Minghua Shen
Presenter: **Zhenghua Zhou**, Sun Yat-sen University

Poster No.: P27
Paper ID: 217
Paper Title: Artificial Neural Network-based Multi-objective Optimisation Method for GaAs RF Inductors
Author(s): Lingmei Ma, Mark Lu, Xiaotian Song, Wei Yao, Christine Tan, Rong Qian, Liang Wu
Presenter: **Lingmei Ma**, Shanghai Institute of Microsystem and Information Technology

Poster No.: P28
Paper ID: 220
Paper Title: Simulation and Exploration for Multi-Chiplet Systems using Open-Source Tools and Heuristic Algorithm
Author(s): Luming Wang, Fangli Liu, Zichao Ling, Zheqin Cao, Yixin Xuan, Jianwang Zhai, Kang Zhao
Presenter: **Luming Wang**, Beijing University of Posts and Telecommunications

Poster No.: P29
Paper ID: 247
Paper Title: Fully Pipelined Sparse Polynomial Multiplication for CRYSTALS-Dilithium
Author(s): Zhengwei Wang, Yijun Cui, Bei Wang, Fei Lyu, Chenghua Wang, Weiqiang Liu
Presenter: **Zhengwei Wang**, Nanjing University of Aeronautics and Astronautics

MEMO

SEMITRONIX

EDA Software and Parametric Tester Supplier

Semitronix Corporation is a leading supplier of characterization and yield improvement solutions encompassing software, hardware, and services for the semiconductor industry, which has numerous successful cases covering multiple integrated circuit process nodes.

For Foundry, we support for full technology life-cycle (from technology definition to mass production) characterization test chip needs. Our PCell based on methodology, addressable IP & design software, product based on design automation solutions and high-speed parametric testers all help our customers drive highly efficient TD learning and achieve higher product yield.

For Design House, we provide with customized test chip solutions to help improve product design for manufacturability, performance, yield and time to market.

Service Advantages:

- Shortening the design-to-market cycle for chip products
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- Lowering development costs and enhancing production efficiency
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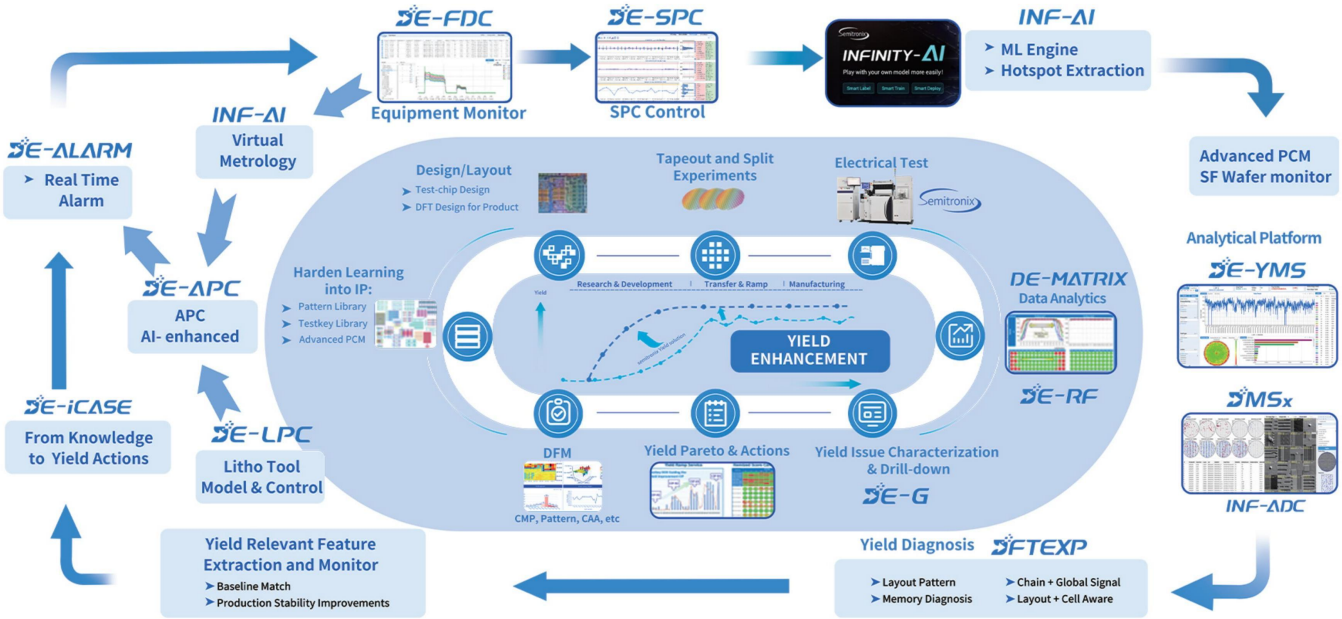

Testchip Design Software:

SmtCell/TCMagic/ATCompiler/Dense Array/ ICSpider: These EDA tools for test chips assist in determining the optimal manufacturing processes and identifying factors affecting yield.

Data Analytics:

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DFTEXP: An automated design-for-testability and yield diagnostic solution

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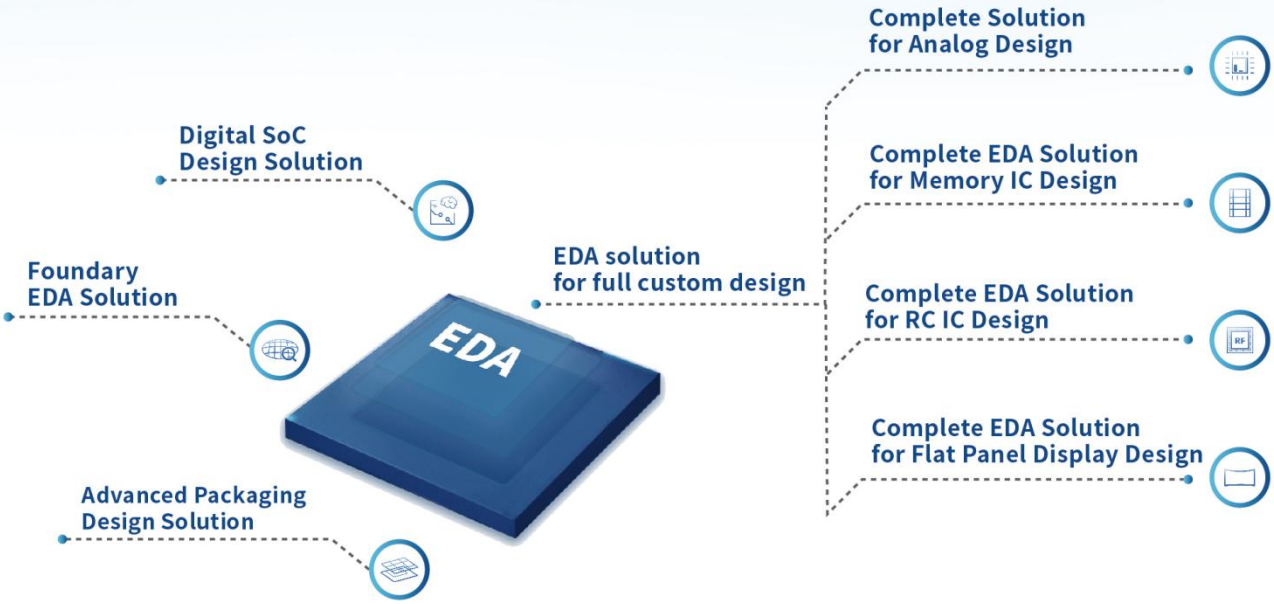
Accelerate Design Success



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- **Digital Verification Full Flow**
  - Verification Hardware Platform: Hyperscale Emulator – UVHP, Unified Verification Hardware System – UVHS
  - PHINE DESIGN Advanced Solo Prototyping Platform Integrated with AMD Versal™ Premium VP1902 Adaptive SoC – PD-AS
  - Virtual Prototyping Kit – UniVista V-Builder/vSpace
  - Digital Simulator – UVS, Debugger – UVD, Verification Productivity System – VPS
- **Digital Implementation**
  - DFT Platform – UniVista Tespert BSCAN/MBIST/ATPG/DIAG/YIELD
- **AI Platform**
  - AI Platform for Digital Design – UniVista Design Assistant

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- PCIe Gen5 IP
- Chiplet Interface: UCIE IP, IO Die Solution
- Ethernet, FlexE, Interlaken Controller IP
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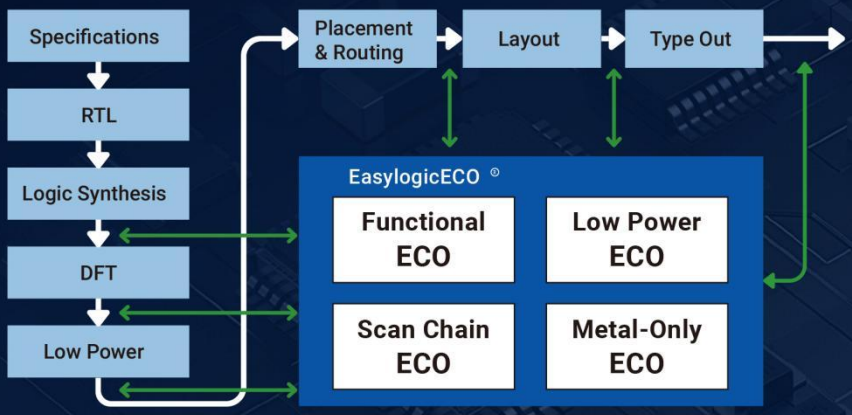

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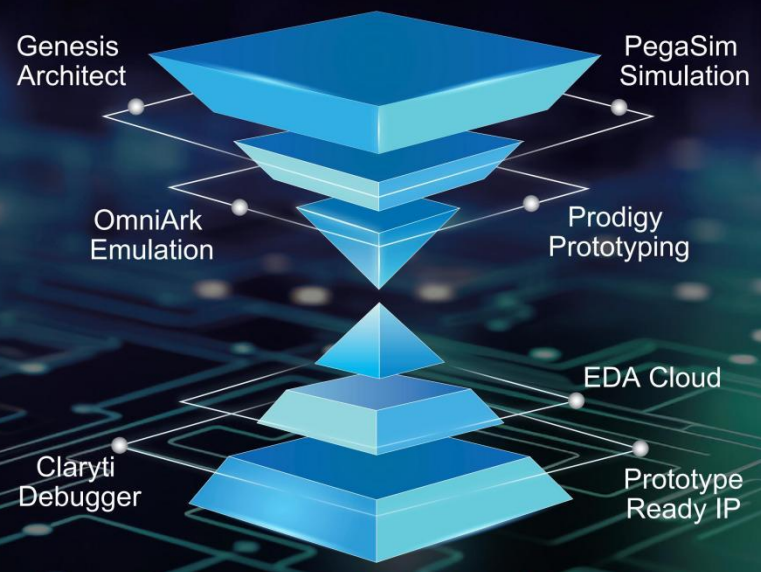

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Paving the Way to Digital Innovation

Xpeedic EDA Overview

From Chip to System

System

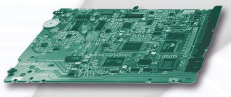
Infrastructure/terminals, Data centers, Automotives

Multi-physics simulation including EM/Thermal/ Stress analysis, System-level verification

Interconnection

System(Infrastructure/terminals, Data centers, Automotives), Connectors/ cables/fibers and other arbitrary interconnection structures

3D full-wave EM simulation, Electrical performance post simulation



PCB

PCB System (Infrastructure/terminals, High-performance computing and Storage, Network switching and routing)

Signal/Power Integrity, Multi-physics simulation including EM/Thermal/Stress analysis, System-level verification

Module

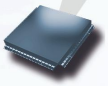
RF devices/modules, Power devices, Optical modules, antennas, Decoupling capacitors design

Signal/Power Integrity, Multi-physics simulation including EM/Thermal/Stress analysis, System-level verification

Package

Conventional/Advanced packaging (SiP, 2.5D/3D, Chiplet heterogeneous integration) design

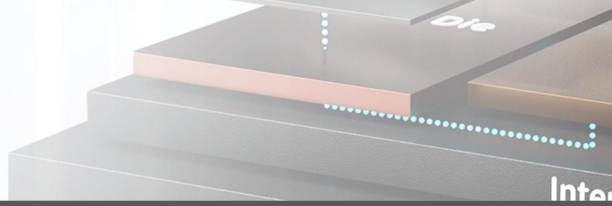
Signal/Power Integrity design, Multi-physics simulation including EM/Thermal/Stress analysis



Chip

Analog/RF Chip Design on Silicon/ Compound Semiconductor Processes

Passive PDK generation, EM simulation, Spice circuit simulation, and Circuit-EM co-simulation



STCO

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Xpeedic is a leading EDA provider to accelerate designs and simulations of next generation high-frequency, high-speed intelligent electronic products. Powered by its proprietary electromagnetic, circuit, and multi-physics solver technologies, Xpeedic is addressing challenges in designing IC in advanced nodes, 3D-IC with advanced packaging, high-speed digital, and RF systems for the markets including data center, automotive, communication, mobile, and IoT. Founded in 2010, Xpeedic has offices in both US and China. For more information, please visit www.xpeedic.com.

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