ISEDA 2024

May 10-13, 2024

Xi'an, China

International Symposium of EDA

CONFERENCE PROGRAM

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[2] Analog Circuit

Chair:

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[3] Digital Design & Verification

Chair:

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[4] Physical Implementation

Chair:

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[5] Wafer Manufacturing

Chair:

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[6] Packaging & Multi-Physics

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[7] Emerging Technologies

Chair:

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[8] EDA Foundation & Standards

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E^2 Uninova Technology

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China Electronics Standardization Institute

[8] Open Source EDA

Chair:

Huawei Li
Institute of Computing Technology, CAS

Co-Chair:

Guojie Luo
Peking University

[8] EDA Contest

Chair:

Longxing Shi
Southeast University

Co-Chair:

Zhixiong Di
Southwest Jiaotong University

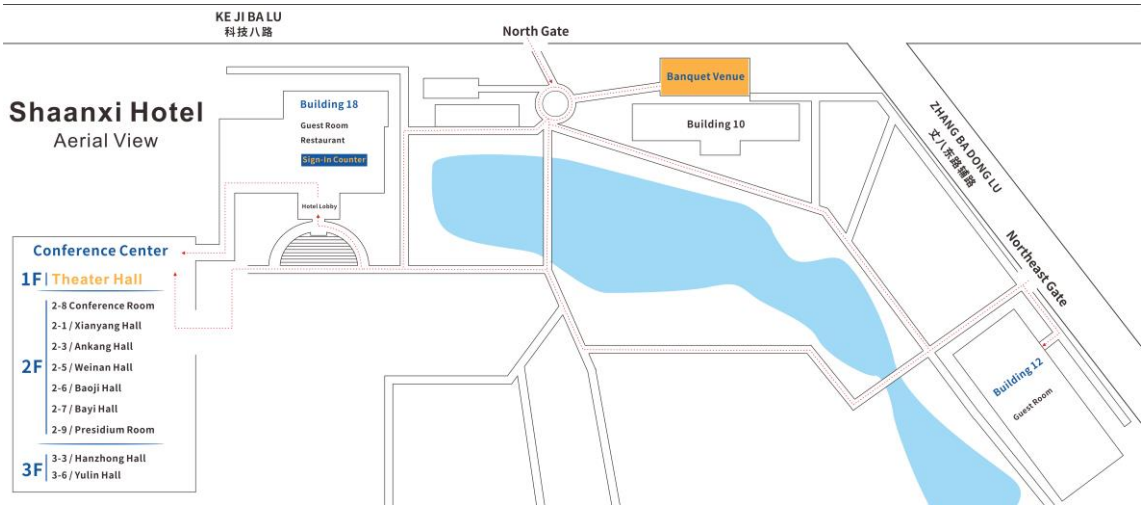
CONFERENCE VENUE

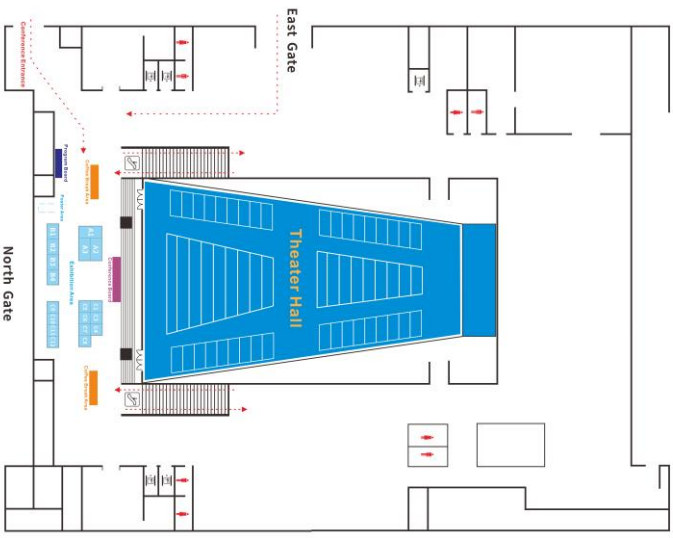
Grand Shaanxi Hotel

Address: No. 1 Zhangba North Road, Yanta District, Xi'an, Shaanxi

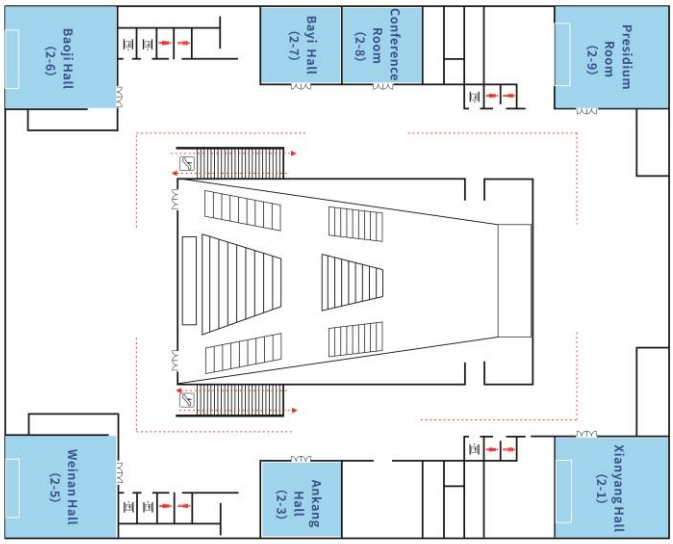
CONFERENCE ROOMS

Meeting Room	May 10	May 11	May 12	May 13
Bld. 18 Room 2-17	★	★		
Theater Hall		★	★	★
2-1 / Xianyang Hall	★	★	★	★
2-3 / Ankang Hall	★	★	★	★
2-5 / Weinan Hall	★	★	★	★
2-6 / Baoji Hall	★	★	★	★
2-7 / Bayi Hall	★	★		
2-8 Conference Room			★	
2-9 / Presidium Room	★	★	★	★
3-3 / Hanzhong Hall	★	★	★	★
3-6 / Yulin Hall	★	★	★	★

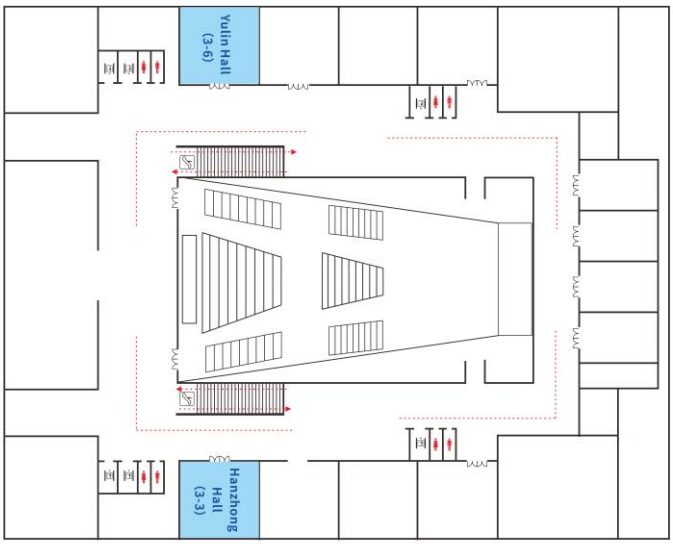




Conference Center 1F



Conference Center 2F



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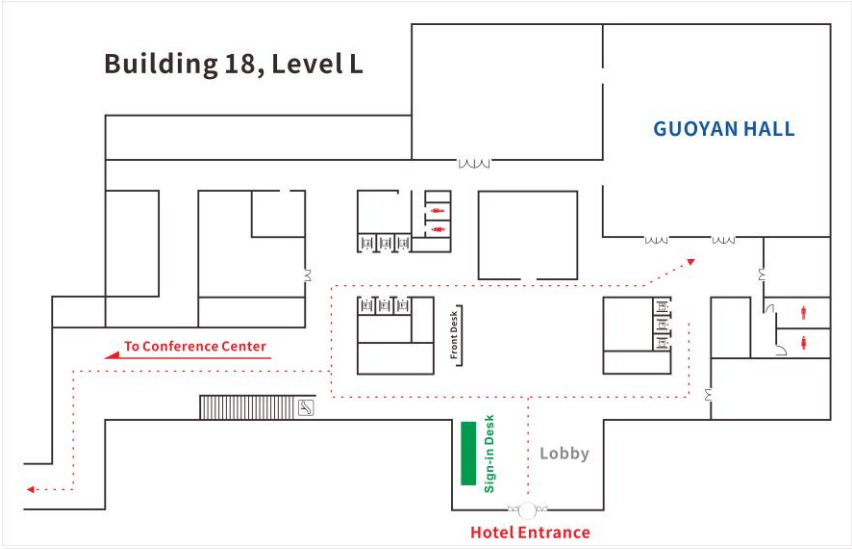
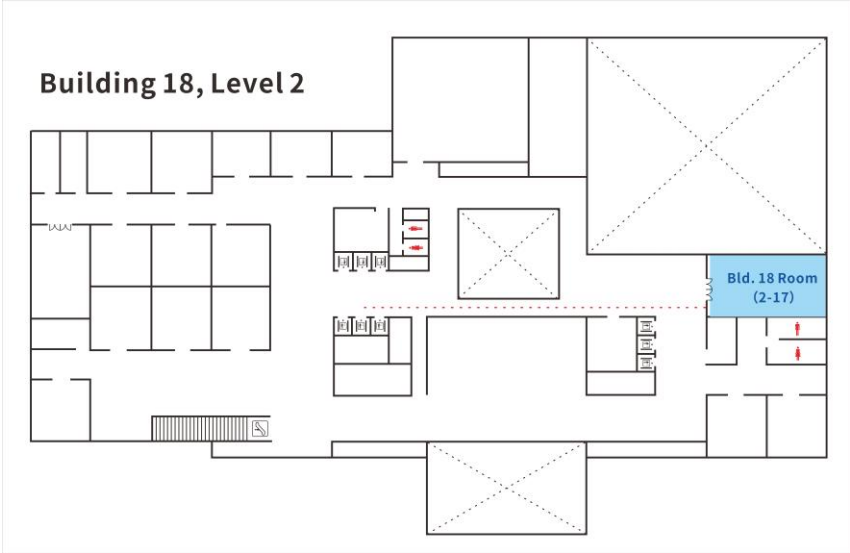
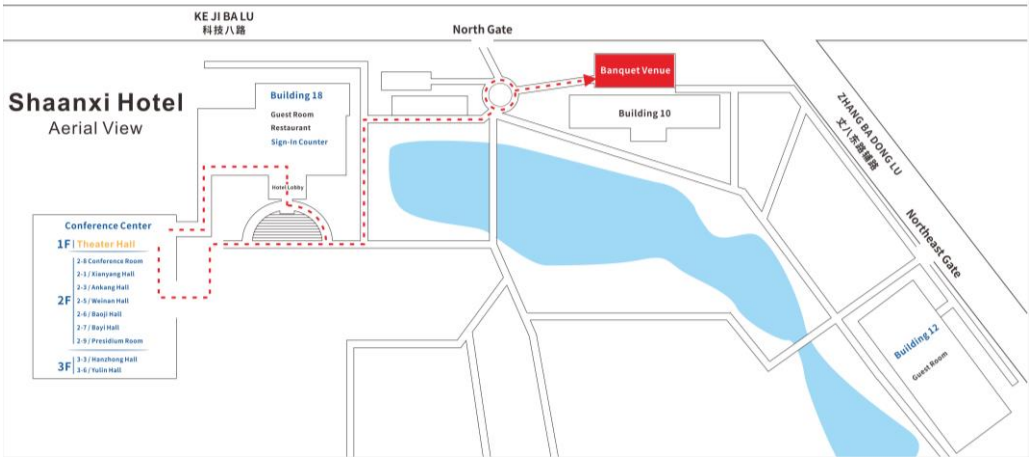

Building 18, Level L
GUOYAN HALL
To Conference Center
Front Desk
Sign-in Desk
Lobby
Hotel Entrance


Building 18, Level 2
Bld. 18 Room
(2-17)


KE JI BA LU
科技八路
North Gate
Banquet Venue
Shaanxi Hotel
Aerial View
Building 18
Guest Room
Restaurant
Sign-in Counter
Building 10
ZHANG BA DONG LU
Northeast Gate
Conference Center
1F Theater Hall
2F
3F
Building 12
Guest Room

AGENDA OVERVIEW

Sign-in & Conference Materials Collection	May 10-13 | 09:00-18:00 Lobby at Bld. 18 of Grand Shaanxi Hotel

May 10, 2024 | Friday		
Time	**Activity**	**Venue**
14:00-17:00	**Workshop (Invited Only):** EDA^2 Technical Roadmap	Bld. 18 Room 2-17
14:00-17:00	**Tutorial 01:** Test and Health Monitoring under Approximations and Variations	3-3 / Hanzhong Hall
14:00-17:00	**Tutorial 02:** Design Automation of Analog Circuits	2-9 / Presidium Room
14:00-17:00	**Tutorial 03:** Agile Design Tools for In-Memory Computing Systems: from Macro Circuit to Architecture	2-3 / Ankang Hall
14:00-17:00	**Tutorial 04:** Boolean Satisfiability Solving, State-of-the-Art	3-6 / Yulin Hall
14:00-17:00	**Tutorial 05:** Benchmarks for 2023 Integrated Circuit EDA Elite Challenge	2-7 / Bayi Hall
14:00-17:00	**Tutorial 06:** Enabling Large Language Models in EDA	2-6 / Baoji Hall
14:00-17:00	**Tutorial 07:** iEDA: An Open-source Physical Design EDA Infrastructure and Toolchain	2-5 / Weinan Hall
14:00-16:30	**Tutorial 08:** Introducing Building Blocks of DTCO	2-1 / Xianyang Hall
14:00-14:45	**Tutorial 09:** Chip Verification Solution Based on Formal Verification	Network Security Bld. Room 713 Xidian University (South Campus)
14:00-17:00	**Tutorial 10:** Application of Chip Verification Solutions	Network Security Bld. Room 708 Xidian University (South Campus)
14:00-16:00	**Tutorial 11:** Training and Demonstration of EDA Tools for the Full Process of RF Circuit Design	Network Security Bld. Room 709 Xidian University (South Campus)
14:00-17:00	**Tutorial 12:** Design Enablement Solution for Novel Semiconductor Devices Research	Network Security Bld. Room 707 Xidian University (South Campus)
18:00	**Dinner @ ISEDA Conference Buffet Points**	

May 11, 2024 | Saturday		
Time	**Activity**	**Venue**
Opening Ceremony Host: **Yu Huang**, HiSilicon Technologies Co., Ltd.		Theater Hall
09:00-09:20	**Ru Huang**, President of Southeast University, Academician of the Chinese Academy of Sciences	
09:20-09:40	**Yue Hao**, Professor of Xidian University, Academician of the Chinese Academy of Sciences	
09:40-09:50	**Hui Chen**, Director of the Xi'an Hi-Tech Industries Development Zone Management Committee	
09:50-10:05	**2023 EDA Contest Award Ceremony**	
10:05-10:10	**Promotion for ISEDA 2025**	
10:10-10:40	**Break @ Foyer of Theater Hall**	
Keynote Speech 1 Host: **Cong Li**, Xidian University		Theater Hall
10:40-11:20	**Jamal Deen**, Distinguished University Professor, McMaster University **Title:** Compact Modeling of Organic/Polymeric Thin Film Transistors for Flexible Electronics	
Keynote Speech 2 Host: **Wenjian Yu**, Tsinghua University		
11:20-12:00	**David Atienza Alonso**, Professor at Embedded Systems Laboratory **Title:** Dynamic Thermal Management and Adaptive Modeling for 3D AI Chips	
12:00-13:30	**Lunch @ ISEDA Conference Buffet Points**	
13:30-15:30	**Technical Session 01:** Latest News From Lithography	2-9 / Presidium Room
13:30-15:50	**Technical Session 02:** The Breakthrough in Testing	2-5 / Weinan Hall
13:30-15:20	**Technical Session 03:** Advanced Tactics in Design Methodology	2-1 / Xianyang Hall
13:30-15:30	**Technical Session 04:** Transient Simulation and Model Reduction	3-3 / Hanzhong Hall
13:30-15:30	**Panel 1:** 2.5D/3D Heterogeneous Integration: Challenges and Opportunities	2-6 / Baoji Hall
13:30-15:30	**Forum:** EDA Contest	3-6 / Yulin Hall
13:00-15:40	**Workshop:** Methods and Challenges in Physical Implementation for 2D and 3D ICs	2-3 / Ankang Hall
15:30-16:00	**Break @ Foyer of Theater Hall**	
15:30-16:00	**Poster Session**	Foyer of Theater Hall
16:00-17:50	**Technical Session 05:** Design Verification	2-6 / Baoji Hall
16:00-18:20	**Technical Session 06:** The Open Source EDA Movement	2-5 / Weinan Hall
16:00-18:20	**Technical Session 07:** Leveraging Machine Learning in EDA	2-1 / Xianyang Hall
16:00-18:20	**Technical Session 08:** Multi-Physics Analysis and Simulation	3-3 / Hanzhong Hall
16:00-18:10	**Technical Session 09:** New Frontiers in Analog EDA	2-9 / Presidium Room
16:00-17:00	**Forum:** EDA Contest	3-6 / Yulin Hall
16:00-17:00	**EDA² Workshop (Invited Only):** Physical Implementation	2-3 / Ankang Hall
13:30-17:30	**EDA² Workshop (Invited Only):** Integration of Industry and Education Working Group Meeting	2-7 / Bayi Hall
13:30-17:30	**Workshop:** Intelligent Circuits: Leveraging AI for Efficient Logic Design and Verification	Bld. 18 Room 2-17
18:00	**Dinner @ ISEDA Conference Buffet Points**	

May 12, 2024 | Sunday		
Time	**Activity**	**Venue**
	Keynote Speech 3 Host: **Qiang Xu**, The Chinese University of Hong Kong	Theater Hall
09:00-09:40	**Xiaoqing Wen**, Professor at Kyushu Institute of Technology **Title:** Power-Aware LSI Testing: Present and Future	
	Keynote Speech 4 Host: **Peter Chun**, University of Alberta	
09:40-10:20	**John Kim**, Professor at Korea Advanced Institute of Science and Technology **Title:** The Hidden Interconnect (or Communication) Challenges	
10:20-10:50	**Break @ Foyer of Theater Hall**	
	Keynote Speech 5 Host: **Fan Yang**, GWX Technology	Theater Hall
10:50-11:30	**Sreejit Chakravarty**, Distinguished Engineer at Ampere Computing **Title:** EDA Challenges in Chiplet Interconnect Test and Repair	
	Keynote Speech 6 Host: **Yunsheng Zheng**, EDA^2	
11:30-12:10	**Christopher Thomas**, Visiting Professor, Tsinghua University & Former Managing Partner, Asia Semiconductor Practice, McKinsey & Company **Title:** Thoughts on the Development of Our Industry	
12:10-13:30	**Lunch @ ISEDA Conference Buffet Points**	
13:30-15:20	**Technical Session 10:** Advanced in EMIR and Parasitic Extraction	3-3 / Hanzhong Hall
13:30-15:30	**Technical Session 11:** Co-Optimizing Systems, Design, and Technology	3-6 / Yulin Hall
13:30-15:10	**Technical Session 12:** Pushing the Envelope in Physical Implementation	2-1 / Xianyang Hall
13:30-15:10	**Technical Session 13:** Design, Safety and Reliability	2-6 / Baoji Hall
13:30-15:20	**Technical Session 14:** Synthesis Techniques: The Next Generation	2-5 / Weinan Hall
13:30-15:20	**Technical Session 15:** Chiplet and 3DIC Revolution & High-Level Synthesis Frontier	2-9 / Presidium Room
15:30-16:00	**Break @ Foyer of Theater Hall**	
16:00-18:00	**Panel 2:** LLM for Chip Design: Challenge and Opportunities	2-6 / Baoji Hall
16:00-18:00	**Panel 3:** The Future of Analog CAD: Navigating the Spectrum between Full Automation and Human Expertise	2-5 / Weinan Hall
16:00-18:00	**Panel 4:** When Math Meets EDA: A Tale of Two Disciplines	2-1 / Xianyang Hall
16:00-18:10	**Technical Session 16:** Memory Testing and Yield Enhancement	2-9 / Presidium Room
16:00-18:20	**Technical Session 17:** EDA Strategies for FPGA Deployment	3-6 /Yulin Hall
16:00-18:10	**Technical Session 18:** Emerging Horizons in TCAD	3-3 / Hanzhong Hall
13:30-17:30	**EDA^2 Workshop (Invited Only):** Technology & Model	2-3 / Ankang Hall
13:30-17:30	**Workshop:** Hardware and Software Co-design for AI Manufacture EDA	2-8 Conference Room
18:30	**Banquet @ Annex of Bld. 10**	

May 13, 2024 | Monday		
Time	**Activity**	**Venue**
	Keynote Speech 7 (Online) Host: **Lining Zhang**, Peking University	Theater Hall
09:00-09:40	**Elyse Rosenbaum**, Professor at University of Illinois **Title:** Circuit Simulation of Integrated Circuit Response to ESD	
	Keynote Speech 8 Host: **Xiaojing Su,** University of Chinese Academy of Sciences	
09:40-10:20	**Jacky Ni**, Founder /CEO of Advanced Manufacturing EDA Co., Ltd. **Title:** Manufacturing EDA in the Era of Generative AI	
10:20-10:40	**Break @ Foyer of Theater Hall**	
	Keynote Speech 9 Host: **Fanjin Meng,** Shanghai Yichip Electronic Technology Co., Ltd.	Theater Hall
10:40-11:20	**Sa Zhao**, Vice President of Engineering in Semitronix Corporation **Title:** Effective Yield Diagnosis – Bridging Design & Manufacturing	
	Keynote Speech 10 Host: **Mingxuan Yuan**, Huawei Noah's Ark Lab	
11:20-12:00	**Han Yu**, Marketing Cooperation Director of Empyrean Technology **Title:** Recent Progress of AI Algorithms for EDA	
	Keynote Speech 11 (Online) Host: **Xin Li**, Duke Kunshan University	
12:00-12:30	**Mehdi B. Tahoori**, Professor at KIT (Karlsruhe Institute of Technology) **Title:** Printed Computing: Design Automation and Computing based on Additive Printed Electronics	
12:30-13:30	**Lunch @ ISEDA Conference Buffet Points**	
13:30-15:10	**Technical Session 19:** The Future of Placement	2-6 / Baoji Hall
13:30-15:10	**Technical Session 20:** Design Space Exploration	3-6 / Yulin Hall
13:30-15:10	**Technical Session 21:** Innovative Pathways in Routing	2-1 / Xianyang Hall
13:30-15:40	**Technical Session 22:** Exploring EDA Applications in HPC and AI	3-3 / Hanzhong Hall
13:30-15:10	**Technical Session 23:** Revolutionizing Timing Analysis	2-9 / Presidium Room
13:30-15:10	**Technical Session 24:** Thermal Management at Chip Level	2-5 / Weinan Hall
15:30-16:00	**Break @ Foyer of Theater Hall**	
16:00-18:00	**Technical Session 25:** Device Simulation and Optimization	2-6 / Baoji Hall
16:00-18:10	**Technical Session 26:** Need More Acceleration? Use FPGA!	2-5 / Weinan Hall
16:00-18:10	**Technical Session 27:** Analog Insights: New Waves on Simulation and Analysis	2-1 / Xianyang Hall
16:00-18:10	**Technical Session 28:** Mastering Synthesis Optimization	2-9 / Presidium Room
16:00-18:10	**Technical Session 29:** Process Modeling and Simulation in Modern Era	3-3 / Hanzhong Hall
16:00-18:00	**Technical Session 30:** Compact Modeling for Circuit Innovation	3-6 / Yulin Hall
13:30-17:30	**EDA^2 Workshop (Invited Only):** Analog Circuit	2-3 / Ankang Hall
18:00	**Dinner @ ISEDA Conference Buffet Points**	

KEYNOTE SPEAKER

Jamal Deen

10:40-11:20 | May 11, 2024
Theater Hall

Distinguished University Professor, McMaster University

Biography: Dr. M. Jamal Deen is Distinguished University Professor (highest rank of a Professor in Canada) and Director of the Micro- and Nano-Systems Laboratory, McMaster University. As an educator, he won the Ham Education Medal from IEEE Canada (highest award for educators), the McMaster University President's Award for Excellence in Graduate Supervision, and MSU Macademics' Lifetime Achievement Award for his exceptional dedication to teaching and significant contribution to student life, the community at large, and academia (highest award for exceptional lifetime teaching at McMaster University voted by the students).

Dr. Deen served as the elected President of the Academy of Science, The Royal Society of Canada in 2015-2017. Currently, he is serving as the inaugural elected Vice President (North) of The World Academy of Sciences, representing the developed countries. His current research interests are nanoelectronics, optoelectronics, nanotechnology, data analytics and their emerging applications to health and environmental sciences. Dr. Deen's research record includes more than 930 peer-reviewed articles (about 20% are invited), two textbooks on "Silicon Photonics- Fundamentals and Devices" and "Fiber Optic Communications: Fundamentals and Applications", 12 awarded patents of which 6 were extensively used in industry, and twenty-six best paper/poster/presentation awards.

As an undergraduate student at the University of Guyana, Dr. Deen was the top ranked mathematics and physics student and the second ranked student at the university, winning the Chancellor's gold medal and the Irving Adler prize. As a graduate student, he was a Fulbright-Laspau Scholar and an American Vacuum Society Scholar. He is a Distinguished Lecturer of the IEEE Electron Device Society for more than two decades now. His awards and honors include the Callinan Award as well as the Electronics and Photonics Award from the Electrochemical Society; a Humboldt Research Award from the Alexander von Humboldt Foundation; the Eadie Medal from the Royal Society of Canada; McNaughton Gold Medal (highest award for engineers), the Fessenden Medal and the Gotlieb Computer Medal, all from IEEE Canada. In addition, he was awarded the five honorary doctorate degrees in recognition of his exceptional research, scholarly and educational accomplishments, exemplary professionalism and valued services. Dr. Deen has also been elected Fellow status in thirteen national academies and professional societies including The Royal Society of Canada - The Academies of Arts, Humanities and Sciences (the highest honor for academics, scholars and artists in Canada), the Chinese Academy of Sciences (China's highest national honor in the area of science and technology and highest academic title), the Canadian Academy of Engineering, IEEE, APS (American Physical Society) and ECS (Electrochemical Society). He was also elected to the Order of Canada, the highest civilian honor awarded by the Government of Canada.

Title: Compact Modeling of Organic/Polymeric Thin Film Transistors for Flexible Electronics

Abstract: In the couple of few decades, the field of flexible organic/polymeric electronics has advanced significantly. This has been primarily because of the developments of new materials, improvements in the quality organic/polymeric materials, as well as the processing techniques, technologies and device designs. For example, roll-to-roll, sheet-to-sheet or printing technologies are being proposed as suitable manufacturing candidates because they can be carried out at room temperature, do not require the kind of clean room environment needed for traditional semiconductor manufacturing, and are very suitable for very low-cost, high volume production. Further, these advances are mostly stimulated by the promise of lighter and more robust devices and systems for applications that include large-area electronics, active matrix large-area displays, large-area solar cells,

KEYNOTE SPEAKER *Continued*

interactive displays, and conformable sensors and actuators. However, despite these advances, there remain challenges in the large-scale transfer of research prototypes into manufactured products. Furthermore, a major the limitation is the lack of accurate and computationally efficient compact models for organic/polymeric thin film transistors with associated parameter extraction techniques. In this presentation, we will discuss recent compact models and illustrate the merits and limitations of several of them as part of the electronic design automation platform. In this presentation, we will discuss our progress in developing industry-viable static and dynamic compact models for flexible transistors with predictable performance and the associated parameter extraction schemes including evolutionary computation for parameter extraction. Finally, we will present several on-going modeling challenges including illumination, hysteresis and contacts effects, as well as models that can predict stability, reliability, and lifetime.

David Atienza Alonso

11:20-12:00 | May 11, 2024
Theater Hall

Professor at Embedded Systems Laboratory, EPFL

Biography: David Atienza Alonso is a professor of Electrical and Computer Engineering, Head of the Embedded Systems Laboratory (ESL) and Scientific Director of the EcoCloud Sustainable Computing Center at EPFL, Switzerland. He received his MSc and Ph.D. degrees in computer science and engineering from UCM, Spain, and IMEC, Belgium, in 2001 and 2005, respectively. His research interests include system-level design methodologies for high-performance multi-processor system-on-chip (MPSoC) and low-power Internet-of-Things (IoT) systems, including new 2-D/3-D thermal-aware design for MPSoCs and many-core servers, ultra-low power edge AI architectures for wireless body sensor nodes and smart embedded systems, HW/SW reconfigurable systems, dynamic memory optimizations, and network-on-chip design. He is a co-author of more than 400 papers, two books, and has 14 licensed patents in these topics. He served as DATE General Chair and Program Chair, and is currently Editor-in-Chief of IEEE TCAD. Among others, Dr. Atienza has received the ICCAD 2020 10-Year Retrospective Most Influential Paper Award, the 2018 DAC Under-40 Innovators Award, and an ERC Consolidator Grant. He is a Fellow of IEEE, a Fellow of ACM, served as IEEE CEDA President (period 2018-2019) and in the IEEE CASS BoG, and is currently the Chair of the European Design Automation Association (EDAA).

Title: Dynamic Thermal Management and Adaptive Modeling for 3D AI Chips

Abstract: The soaring demand for computing power in this AI era has produced as collateral undesirable effects a surge in power consumption and heat density for computing systems. With the rising cooling costs and challenges in heat removal in the latest nano-scale and heavily heterogeneous multi-processor system-on-chip (MPSoC) designs targeting the execution of the latest generative AI algorithms, the development of accurate but fast thermal modeling frameworks to develop dynamic thermal management (DTM) approaches have become indispensable.

These new approaches strongly depend on the availability of efficient and scalable methodologies for thermal and power modeling, analysis, and characterization of computing systems at multiple abstraction levels. These methodologies must provide the appropriate accuracy to capture the thermal diffusion mechanisms in 2D and 3D AI chips and fast adaptation for the design space exploration of MPSoCs architectures and the latest cooling technologies. In this talk, Prof. Atienza will review the basis of the recent innovative thermal modeling and prototyping approaches for non-uniform thermal characterization included in the open-source 3D Interlayer Cooling Emulator (3D-ICE). Then, in conjunction with a fast offline application profiling strategy utilizing gem5-X, the latest open-source architecture simulator for 2D/3D MPSoCs designs targeting AI chips, it will be shown

KEYNOTE SPEAKER *Continued*

how it is possible to develop a complete DTM evaluation framework that can be used to create Multi-Agent Reinforcement Learning (MARL) control schemes for different 3D MPSoCs and AI accelerators. Finally, it will be illustrated how this DTM framework based on MARL control can support advanced liquid cooling and electricity-generation technologies using microfluidic power cells for the next generation of energy-efficient 2D and 3D AI accelerators.

Xiaoqing Wen

09:00-09:40 | May 12, 2024
Theater Hall

Professor at Kyushu Institute of Technology

Biography: Xiaoqing WEN received the B.E. degree from Tsinghua University, China, in 1986, the M.E. degree from Hiroshima University, Japan, in 1990, and the Ph.D. degree from Osaka University, Japan, in 1993. He was an Assistant Professor at Akita University, Japan, from1993 to 1997, and a Visiting Researcher at the University of Wisconsin–Madison, USA, from Oct. 1995 to Mar. 1996. He joined SynTest Technologies Inc., USA, in 1998, and served as its Vice President and Chief Technology Officer until 2003. He joined Kyushu Institute of Technology, Japan, in 2003, where he is currently a Professor with the Department of Computer Science and Networks. He is a Co-Founder and Co-Chair of Technical Activity Committee on Power-Aware Testing under Test Technology Technical Council (TTTC) of IEEE Computer Society. He is serving as Associate Editors for IEEE Transactions on Very Large Scale Integration Systems (TVLSI) and Journal of Electronic Testing: Theory and Applications (JETTA). He co-authored and co-edited the latest VLSI test textbook in 2006 and the first comprehansive book on power-aware VLSI testing in 2009. His research interests include design, test, and diagnosis of LSI circuits. He has published more than 300 papers and holds 43 U.S. patents & 14 Japan patents. He received the 2008 Society Best Paper Award from IEICE-ISS. He is a Fellow of IEEE.

Title: Power-Aware LSI Testing: Present and Future

Abstract: With low power consumption becoming a key requirement for advanced LSI designs, the gap between functional power and test power has kept growing to such an extent that power-aware testing has now become a must. The foundation of power-aware testing is a complete understanding of the global impact of switching activity on peak and average power as well as the local impact of switching activity on IR-drop-induced delay increase along data and clock paths. This talk presents a holistic view on various aspects of power-aware testing, aimed at helping researchers and engineers to develop more sophisticated and complete solutions for controlling LSI test power.

John Kim

09:40-10:20 | May 12, 2024
Theater Hall

Professor at (KAIST) Korea Advanced Institute of Science and Technology

Biography: John Kim is currently a full professor in the Schoolof Electrical Engineering at KAIST (Korea Advanced Institute of Science and Technology) in Daejeon, Korea. John Kim received his Ph.D. from Stanford University and

KEYNOTE SPEAKER *Continued*

B.S/M.Eng from Cornell University. His research interests include computer architecture, interconnection networks, security, and mobilesystems. He has received a Google Faculty Research Award, Microsoft-Asia New Faculty Fellowship, and is listed in the Hall of Fame for ISCA, MICRO, and HPCA. He has also worked on the design of several microprocessors at Intel and at Motorola.

Title: The Hidden Interconnect (or Communication) Challenges

Abstract: As compute and memory continue to scale, the interconnect or the communication is becoming a critical bottleneck in determining overall system performance and scalability. In this talk, I will present the challenges of the "hidden" interconnect that exists in modern systems in terms of its impact on the design, performance, reliability/security, and cost of the system. In particular, I will present case studies from recent interconnect architectures.

Sreejit Chakravarty

10:50-11:30 | May 12, 2024
Theater Hall

Distinguished Engineer at Ampere Computing

Biography: Dr. Sreejit Chakravarty is an IEEE Fellow, a highly recognized Researcher, Inventor, and a Distinguished Engineering Leader, with extensive industry and academic experience. He is currently a Distinguished Engineer at Ampere Computing, Santa Clara, CA, USA where he drives the strategic initiatives for product quality. Prior to this, he had over 25 years of industry experience as a Principal Engineer with Intel Corporation and Distinguished Engineer at LSI and AVAGO. He started his career in academia as an Associate professor of Computer Science, at The State University of New York at Buffalo, where his work was funded by multiple National Science Foundation Grants. He has architected innovative solutions across the entire silicon life cycle spanning Silicon Quality and Reliability (RAS, Functional Safety and Silent Data Errors) and subsequently drove them from concept to product intercept. He has published 1 book, authored 145+ IEEE papers, has 23 issued US patents, graduated several doctoral students, served in various capacities at numerous IEEE conferences, and delivered multiple keynote addresses. He has mentored research at several universities like Princeton, USC, UIUC, etc. For his professional work, he has been recognized as an IEEE Fellow and SUNY Distinguished Alumni. He currently chairs the IEEE Study Group on Chiplet Interconnect Test and Repair, which aims to standardize the test and repair of chiplet interconnects which will lay the foundation to realize the chiplet revolution.

Title: EDA Challenges in Chiplet Interconnect Test and Repair

Abstract: Chip-let based design is here to stay and, fueled by various advanced packaging technologies, it is projected to revolutionize the semiconductor industry. This talk will discuss the following:

(i) the interconnect test and repair problem;

(ii) the need for and the ongoing effort, under IEEE P3405, to standardize interconnect test and repair; and

(iii) EDA challenges in accomplishing a standardized interconnect test and repair solution.

Christopher Thomas

11:30-12:10 | May 12, 2024
Theater Hall

Visiting Professor, Tsinghua University & Former Managing Partner, Asia Semiconductor Practice, McKinsey & Company

Biography: Chris Thomas was most recently a partner with McKinsey & Company. He served as co-Managing Partner for the Firm's Global Digital Strategy service line as well as its Global IoT service line; and as the leader of its Asia Semiconductor Practice. Prior to McKinsey, Chris spent ten years at Intel. He was the General Manager of Intel China, with joint ownership for the region's $5 billion-plus P&L. In this role, he grew revenues by more than 50% and oversaw China's successful elevation from a sales unit to an independent regional P&L business reporting directly into headquarters. He also led several business units in the Silicon Valley headquarters. Chris began his career as a private equity investor at The Blackstone Group in New York City. Chris is a Visiting Professor at Tsinghua University, China's leading educational institution. He received an MBA from Stanford Business School, where he was an Arjay Miller scholar; a Master of Arts in Political Science from Stanford University; and a Bachelor of Science in Economics, summa cum laude, from the Wharton School.

Title: Thoughts on the Development of Our Industry

Abstract: Christopher Thomas will share his views on the long-term evolution of the semiconductor industry, including the impact of AI, new applications, government policies, geopolitical competition, new market entrants, and more. He will share key questions and inflection points that will determine the future of our industry.

Elyse Rosenbaum

09:00-09:40 | May 13, 2024
Theater Hall
(Online)

Professor at University of Illinois

Biography: Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois Urbana-Champaign. She received a Ph.D. in electrical engineering from University of California, Berkeley. She is the director of the Center for Advanced Electronics through Machine Learning (CAEML), a joint project of the University of Illinois, North Carolina State University, and Penn State University. Her current research interests include CDM-ESD reliability, ESD-robust high-speed I/O circuit design, compact modeling, optimization of heterogeneously integrated system-in-package, and machine learning aided modeling of circuit lifetime distributions.

Dr. Rosenbaum has authored or co-authored over 200 technical papers; she has been an editor for IEEE Transactions on Device and Materials Reliability and IEEE Transactions on Electron Devices. She served as the General Chair of the 2018 International Reliability Physics Symposium. Dr. Rosenbaum was the recipient of a Best Student Paper Award from the IEDM, an Outstanding Paper Award and 2 Best Paper Awards from the EOS/ESD Symposium, a Technical Excellence Award from the SRC, an NSF CAREER award, an IBM Faculty Award, and the ESD Association's Industry Pioneer Recognition Award. She is a Fellow of the IEEE.

Title: Circuit Simulation of Integrated Circuit Response to ESD

Abstract: ESD protection circuits degrade circuit performance and/or consume valuable Si area. Thus, a conservative approach to ESD device sizing is undesirable. To avoid ESD overdesign without compromising the ability to meet ESD specifications on the first silicon spin requires that ESD designs be validated by circuit simulation. In this talk, I will describe some of the compact models used for ESD simulations and present various case studies.

Jacky Ni

09:40-10:20 | May 13, 2024
Theater Hall

Founder /CEO of Advanced Manufacturing EDA Co., Ltd.

Biography: Jacky Ni, founder and CEO of Advanced Manufacturing EDA Co., Ltd. (AMEDAC). Mr. Ni dedicated in EDA development for more than 20 years with a wealth of experience and contribution in the China EDA industry, and used to be experienced in EDA product innovation, market development, corporate strategy and management, etc.. Prior to AMEDAC, Mr. Ni served as Deputy General Manager of Synopsys China, a global leading EDA company. During his more than 13-year tenure at Synopsys, Mr. Ni was used responsibility for corporate strategy and implementation, product planning and development, R&D management, sales operations and product application. Mr. Ni successfully boosted the market share of Synopsys in the field of Foundry Business in China, and used to serve multiple leading companies across the IC value chain and end application firms. Since Mr. Ni started to lead Synopsys China Foundry Business, he and his team were honored with excellent supplier award of important clients including SMIC's 28nm Outstanding Contribution Award, that proved the industry's recognition of Mr. Ni's contribution. After Synopsys, as COO of Alchip (a famous chip design service company), Mr. Ni successfully repositioned the company as the leader in AI chip design service, by refining the strategy and vision of Alchip, transforming the corporate organization to improve efficiency and lead business innovation. Mr. Ni founded AMEDAC in 2019. Utilizing his management practice and extensive network in the EDA field, Mr. Ni has led AMEDAC to be the first supplier to provide self-developed manufacturing EDA software, which solves the most important technical shortcomings of domestic EDA. Mr. Ni along with this 5-year-old company, has covered full flow EDA tools for advanced chip manufacturing, and moves a big step towards intelligence integration of EDA.

Title: Manufacturing EDA in the Era of Generative AI

Abstract: Generative AI represented by LLM has demonstrated excellent and versatile solution capabilities. It has proven useful in a range of applications and the EDA field has begun to rapidly adopt the LLM model recently. The evolution of EDA has been accerlated by generative AI technologies, and the cutting-edge technolohgy has shown its contribution to many field, including large-scale data process, engineering effciency improvement, work flow integration, etc., which reveals Generative AI's transformative power on chip design and implementation.

As chip shrinking, structures becoming more complex, and 3D-IC developing, manufacturing EDA plays more important role in the value chain. The implementation of manufacturing EDA is based on entensive professional data and experience, various mathematical and physical algorithms, which is consistent with the core value of LLM. Thus, we have seen many application of generative AI in the field of manufacturing EDA, including ViT in patterning, LLM in smart manufacturing and LLM using for manufacturing flow integration. Further, some of the most cutting-edge developments demonstrate the potential of generative AI to integrate the entire process from design to manufacturing to 3D advanced packaging, that could change the EDA development model.

We have moving a step on explore generative AI in manufacturing EDA. Based on the data, knowledge accumulation and our understanding on artificial intelligence embedding in EDA software, we have already achieved good results in fields such as AI copilot in chip manufactruing, AI generating code and AI integrating chip implemention flow. By leveraging generative AI technology, It can realize automatic integrated processes and interconnections from design, process, manufacturing to 3D packaging, thereby greatly improving the efficiency of advanced chip R&D and production.

Sa Zhao

10:40-11:20 | May 13, 2024
Theater Hall

Vice President of Engineering in Semitronix Corporation

Biography: Ms. Sa Zhao received her B.S. in Physics from Peking University and M.S. in Physics from Purdue University. With over 25 years of semiconductor industry experience, Ms. Zhao currently serves as Vice President of Engineering in Semitronix Corporation, focusing on Manufacturing EDA and IC Yield Ramp services. Prior to design houses on yield enhancement, device optimization, DFM technologies, inline control methodologies. Through her visionary leadership and strategic insights, Semitronix pushed the boundaries of conventional yield management & control systems, harnessing the power of AI and ML to unlock new levels of performance and efficiency to enhance product yield, quality, and reliability.

Title: Effective Yield Diagnosis – Bridging Design & Manufacturing

Abstract: In the prevalent foundry-design house eco-system, achieving optimal yield outcome requires close engagement between players.

An integrated data framework is a key enabler for such collaborations, where product and process insights meet. In this talk, we propose a complete work-flow where design-side DFT (design-for-test), diagnostics and product layout features are combined with production data and proprietary fine-grained process monitors to facilitate the efficient identification/quantification of yield drivers and mechanisms.

This understanding, in turn, supports both fab-side production improvements and design-side DFM (design-for-manufacturing) mitigations.

Han Yu

11:20-12:00 | May 13, 2024
Theater Hall

Marketing Cooperation Director of Empyrean Technology

Biography: Yu Han, with the Chinese National Senior Engineer Title, graduated from Beihang University with Master Degree in 2007. He worked for Empyrean Technology Corp. (Empyrean) from 2010 till now. He is now the Senior Technical Marketing Director of Empyrean, leading some business including external technical corporation and university programs. He has published over 10 articles on academic journals such as IEEE-DAC, ACM-GLSVLSI, China Integrated Circuit etc. as the first author. He has also served as a review expert of the "National Project of Micro-Nano Electronics", the deputy director of the editorial board of "National Vocational and Technical Skill Standards - Integrated Circuit Engineering", and the director of Guangdong EDA Engineering Center.

Title: Recent Progress of AI Algorithms for EDA

Abstract: This presentation will show some commercial EDA tool having used AI Algorithm like machine learning and neural network. It will also discuss the possible applications of big language model in EDA field.

Mehdi B. Tahoori

12:00-12:30 | May 13, 2024
Theater Hall
(Online)

Professor at KIT (Karlsruhe Institute of Technology)

Biography: Mehdi B. Tahoori is Professor and the Chair of Dependable Nano-Computing at Karlsruhe Institute of Technology (KIT), Germany. He received the B.S. degree in computer engineering from Sharif University of Technology, Tehran, Iran, in 2000, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2002 and 2003, respectively. He is currently the deputy editor-in-chief of IEEE Design and Test Magazine. He was the editor-in-chief of Elsevier Microelectronic Reliability journal. He was the program and general chair of IEEE VLSI Test Symposium in (VTS) and General Chair of IEEE European Test Symposium (ETS). Prof. Tahoori was a recipient of the US National Science Foundation Early Faculty Development (CAREER) Award in 2008 and European Research Council (ERC) Advanced Grant in 2022. He has received a number of best paper nominations and awards at various conferences and journals. He is currently the chair of IEEE European Test Technologies Technical Council (eTTTC). He is a fellow of the IEEE.

Title: Printed Computing: Design Automation and Computing based on Additive Printed Electronics

Abstract: Printed electronics is an emerging and fast-growing field which can be used in many demanding and emerging application domains such as wearables, smart sensors, and Internet of Things (IoT). Unlike traditional computing and electronics domain which is mostly driven by performance characteristics, printed and flexible electronics based on additive manufacturing processes are mainly associated with low fabrication costs and low energy. Printed electronics offer certain technological advantages over their silicon-based counterparts, such as mechanical flexibility, low process temperatures, maskless and additive manufacturing possibilities. Nevertheless, due to low device count, large feature sizes and high variabilities, originated in low-cost additive manufacturing, existing design automation and computing paradigms of digital VLSI are not applicable to printed electronics. This talk covers the technology, process, modeling, fabrication, design automation, and computing paradigms for circuits and systems based on additive printed technologies.

TUTORIAL

T01. Test and Health Monitoring under Approximations and Variations

Time	14:00-17:00 | May 10, 2024	Venue	3-3 / Hanzhong Hall

ABSTRACT

Process and dynamic variations including voltage and temperature fluctuations, crosstalk interaction or aging effects complicate distinguishing between defects, reliability threats, and benign behavior. New compute paradigms like approximate computing aggravate the problem since they may hide malicious reliability threats. This tutorial introduces into the most recent techniques for offline and online test and health monitoring under variations and presents simulation and test generation techniques to overcome the multi-dimensional variation space.

Case studies show, how error rate monitoring under dynamic voltage/frequency scaling and approximate computing and communication lead to improvements of performance, power consumption and reliability at the same time.

SPEAKER(S):

SPEAKER

Hans-Joachim Wunderlich
University of Stuttgart

Biography: Hans-Joachim Wunderlich is Professor Emeritus of the University Stuttgart and a Life Fellow of IEEE. He received the diploma degree in mathematics from the University of Freiburg, Germany, in 1981 and the Dr. rer. nat. (Ph.D. degree) from the University of Karlsruhe in 1986. Since 1991, he has been a full professor. From 2002 to 2018, he was the director of the Institute of Computer Architecture and Computer Engineering at the University of Stuttgart, Germany. He has been associate editor of various international journals and organizer of a variety of IEEE conferences on design, test and fault tolerance of electronic systems. He has published 15 books and book chapters and around 300 reviewed scientific papers in journals and conferences. His research interests include test, reliability, fault tolerance and design automation of microelectronic systems.

TUTORIAL

T02. Design Automation of Analog Circuits

Chair: Fan Yang, Fudan University

Time	14:00-17:00 | May 10, 2024	Venue	2-9 / Presidium Room

ABSTRACT

Manual design processes are time-consuming and often rely heavily on designers' experiences. Design automation offers a solution by leveraging algorithms and tools to streamline the design process, optimize performance, and reduce the time-to-market. In this tutorial, we will cover the TED system, transistor sizing and physical design algorithms for analog circuits.

SPEAKER(S):

SPEAKER

Zuochang Ye
Tsinghua University

Biography: Zuochang Ye received his Ph.D degree from Tsinghua University in 2007. He has been worked as a research scientist in Cadence Research Laboratories at Berkeley. He is currently an Associate Professor with the School of Integrated Circuits, Tsinghua University. His is mainly working on analog design automation.

Title: TED: A Python-Based Analog Design Environment for Agile Circuit Development

SPEAKER

Liwen Zhuo
Empyrean Technology Co.

Biography: Liwen Zhuo is a senior product manager at Empyrean Technology Co. He has 18 years of experience in the EDA (Electronic Design Automation) industry. His research areas include analog integrated circuit design platform, analog integrated circuit design automation & optimization and intelligent layout & wiring.

Title: pyAether: Fully Customized Design Platform based on Python

SPEAKER

Zhaori Bi
Fudan University

Biography: Bi Zhaori, Assistant Researcher at the State Key Laboratory of Integrated Chips and Systems, Fudan University. Currently engaged in research on analog integrated circuit design automation, development and theoretical research of high-performance computer algorithms, nonlinear optimization theory, and medical artificial intelligence. Dr. Bi obtained his Ph.D. in Computer Engineering from the University of Texas at Dallas in 2017. He is an Associate Editor of the Integration journal and serves as a reviewer for EDA journals such as TCAD, TCAS-II, TBE, and TODEAS.

Title: Analog Circuit Sizing Algorithms

SPEAKER

Keren Zhu
The Chinese University of Hong Kong

Biography: Keren Zhu is currently a research assistant professor in the Department of Computer Science and Engineering at The Chinese University of Hong Kong. In 2022, he received his Ph.D. from the Department of Electrical and Computer Engineering at The University of Texas at Austin, USA. He earned his B.S. in Electrical Engineering with the highest distinction from the University of Wisconsin-Madison, USA, in 2016. Dr. Zhu's research focuses on physical design automation, analog integrated circuit design automation, machine learning for EDA, and computing systems with emerging technologies. During his Ph.D. studies, Dr. Zhu was a key contributor to the development of MAGICAL, an open-source analog layout automation software. He has authored dozens of technical papers on electronic design automation, circuit design, and machine learning, which have been published in leading venues, as well as multiple book chapters. His research has received recognition through nominations for best paper awards at several conferences.

Title: Physical Design of Analog Circuits

TUTORIAL

T03. Agile Design Tools for In-Memory Computing Systems: from Macro Circuit to Architecture

Chair: Chixiao Chen, Fudan University

Time	14:00-17:00 | May 10, 2024	Venue	2-3 / Ankang Hall

ABSTRACT

In-memory computing (IMC) or processing-in-memory (PIM) is an emerging technology for non-Von-Neumman architecutre, where computations are performed directly within the memory itself, rather than being sent to a separate central processing unit (CPU). Thanks to the tight coupling between computing logics and memory designs, IMC's latency and power consumption are much better than traditional architecture. In addtion, leveraging either analog circuit or custim digital gates, IMC also features good energy efficiency. From an Electronic Design Automation (EDA) perspective, however there lacks mature tools to complete a IMC system as agile as traditional digital design. The tutorial provides an overview of the latest advancements in agile compute in memory tools , from macro to architecture level.

The first half of the turial covers an overall introduction for the IMC macro compiler, namely automatic synthesis and physical design tools for IMC macros. A circuit generator and agile placement-and-routing tool for both analog and digital IMC macros is first demonstrated. In addtion, an improved version of robust IMC complier with MBIST is discussed, which supports configuration of integer and floating point modes.

The second half will introduce several architectural level tools for IMS system design. It includes an automatic architecture synthesis tool for generating NVM crossbar-based DNN accelerators, a universal compilation framework for PIM DNN accelerators, and a full-system PIM simulator to facilitate circuit-, architecture- and system-level researches.

SPEAKER(S):

SPEAKER

Chixiao Chen

Fudan University

Biography: Chixiao Chen received the B.S. and Ph.D. degrees in microelectronics from Fudan University, Shanghai, China, in 2010 and 2015, respectively.,In 2015, he worked at Calterah Inc., Shanghai, as an Analog/Mixed Signal Circuit Design Engineer. From 2016 to 2018, he was a Postdoctoral Research Associate with the University of Washington, Seattle, WA, USA. In 2019, he joined Fudan University, where he is currently an Associate Professor with the Frontier Institute of Circuits and Systems. He is also the Director of the Integrated Chips Innovation Center of the State Key Laboratory of Integrated Chips and Systems, Fudan University. His current research interests include mixed-signal integrated circuit design and custom intelligent software–hardware codesigns. He was a recipient of the NSFC Excellent Young Scientists Fund and serve as a TPC Member for A-SSCC.

SPEAKER

Xiaoming Chen

Institute of Computing Technology, CAS

Biography: Xiaoming Chen received the BS and PhD degrees in electronic engineering from Tsinghua University, Beijing, China, in 2009 and 2014, respectively. He is now an associate professor with the Institute of Computing Technology, Chinese Academy of Sciences. His current research interests include design automation for integrated circuits and computer architectures. He has published more than 120 papers in DAC, ICCAD, HPCA, MICRO, ASPLOS, IEEE TCAD, IEEE TC, etc. He was a recipient of the NSFC Excellent Young Scientists Fund, 2016 European Design and Automation Association (EDAA) Outstanding Dissertation Award, 2018 DAMO Academy Young Fellow Award, and ASP-DAC 2022 Best Paper Award.

TUTORIAL

T04. Boolean Satisfiability Solving, State-of-the-Art

Chair: Zhufei Chu, Ningbo University

Time	14:00-17:00 | May 10, 2024	Venue	3-6 /Yulin Hall

ABSTRACT

The Boolean satisfiability (SAT) problem, a fundamental issue in computer science, revolves around determining the existence of an interpretation that satisfies a given Boolean formula, typically represented in conjunctive normal form (CNF). It holds the distinction of being the first problem proven to be NP-complete, highlighting its significance in computational complexity theory.

The realm of SAT solvers has witnessed remarkable growth, with numerous techniques developed and applied across various domains. In fields such as electronic design automation (EDA), SAT-based methodologies play a pivotal role in logic reasoning tasks such as equivalence checking, SAT sweeping, and automatic test pattern generation (ATPG). Conversely, EDA techniques can be harnessed to enhance SAT-solving efficiency through avenues such as circuit-based SAT solvers, logic synthesis, and AI-driven approaches.

In this tutorial, we have planned three talks to address different aspects of SAT problem-solving. Our first session will provide an in-depth exploration of SAT fundamentals and elucidate recent advancements in solving techniques. Following this, our second talk will spotlight the synergy between logic synthesis and AI-driven methodologies in boosting SAT-solving capabilities. Finally, our third session will introduce a novel reasoning engine based on semi-tensor product and circuit-based SAT solvers, offering a fresh perspective on tackling SAT problems.

SPEAKER(S):

SPEAKER

Shaowei Cai

Institute of Software, Chinese Academy of Sciences

Biography: Shaowei Cai is a Professor at Institute of Software, Chinese Academy of Sciences. He received his PhD degree from Peking University with Distinguished Doctoral Dissertation Award. His research interests include constraint solving and formal verification. He proposed a powerful hybrid approach for SAT, which has been widely used in state of the art CDCL solvers. He has received the Best Paper Award at SAT 2021 conference. He has won more than 10 gold medals in SAT and SMT Competitions, and his solvers were ranked 1st many times in MaxSAT Evaluations. He has also led a team working on EDA formal verification tools.

SPEAKER

Qiang Xu

The Chinese University of Hong Kong

Biography: Qiang Xu is a Professor at The Chinese University of Hong Kong, his current research interests include large circuit models, EDA, and AI in general. He has published 180+ papers with 8000+ citations, including several best papers at prestigious conferences and an ICCAD Ten Year Retrospective Most Influential Paper. He has supervised ~20 Ph.D. dissertations and his students have won EDAA Outstanding Dissertation Award and the semi-finals of IEEE TTTC Doctoral Thesis Award.

SPEAKER

Zhufei Chu
Ningbo University

Biography: Zhufei Chu received the B.S. degree in electronic engineering from Shandong University, Weihai, China, in 2008 and the M.S. and Ph.D. degrees in communication and information system from Ningbo University, Ningbo, China, in 2011 and 2014, respectively. He was a Postdoctoral Fellow at the Ecole Polytechnique Fedederale de Lausanne (EPFL) during 2016 to 2017. He is currently a Full Professor at Ningbo University, Ningbo, China. He serves as the proceedings chair (2019-2021) and finance chair (2022-2023) of the international workshop on logic and synthesis (IWLS), technical program chair (2023) of international conference on circuits and systems (ICCS), digital design & verification track chair (2023-2024) of the IEEE international symposium of EDA (ISEDA), and also technical program committee members for design automation conference (DAC), IWLS, and international conference on VLSI design (VLSID). He is actively maintaining the logic synthesis framework ALSO (https://gitee.com/zfchu/also). His current research interests include the many aspects of logic synthesis and its applications.

TUTORIAL

T05. Benchmarks for 2023 Integrated Circuit EDA Elite Challenge

Chair: Zhixiong Di, Southwest Jiaotong University

Time	14:00-17:00 | May 10, 2024	Venue	2-7 / Bayi Hall

ABSTRACT

This tutorial focuses on the benchmarks of the four problems from the 2023 Integrated Circuit EDA Elite Challenge contest. The focus of this tutorial is to showcase the application scenarios, academic value, and future improvement directions of these benchmarks, and to guide the audience to learn how to use these benchmarks through hands-on practice. This tutorial hopes to help more relevant researchers and students conduct academic research and exploration based on these benchmarks.

SPEAKER(S):

SPEAKER

Huan Kan

Semitronix Corporation

Biography: Huan Kan serves as the EDA product director at Semitronix corporation and possesses nearly 20 years of experience within the semiconductor industry. Having held positions at leading domestic IC manufacturing and EDA software companies like SMIC, HLMC and Semitronix corporation, he has served in various roles including Manager of DFM R&D Department and EDA product director. He has led the development of DFM technologies for multiple advanced process nodes, including Finfet processes. He is also one of the primary question setters for the "Ultra-Large Scale Layout Pattern Matching Algorithm" competition problem in the Integrated Circuit 2023 EDA Elite Challenge.

Title: Benchmark for Ultra-Large-Scale Layout Pattern Matching Algorithm

Abstract: Pattern Matching is a type of pattern search technology aimed at rapidly locating specific template shapes within ever-expanding layouts. This technique has been widely adopted in fields such as Design For Manufacturability (DFM), Optical Proximity Correction (OPC), and layout optimization. In this tutorial, we will introduce the technological background of Pattern Matching, common application scenarios, test cases for competition problems, and scoring methods. Additionally, there will be a live demonstration of an outstanding competition entry.

SPEAKER

Zhenghua Qi

X-EPIC Corporation Limited

Biography: Zhenghua Qi is Vice President of X-EPIC CORPORATION LIMITED. He graduated from Fudan University and the University of Colorado. He used to work at Synopsys, engaged in EDA validation product development for more than 20 years. Participated in and took charge of several major strategic projects of the company. Responsible for the establishment of Synopsys China Verification Technology R&D Center. Led and took charge of several major strategic and technical projects. Such as global standard digital emulator (VCS) compiler, UVM industry standard development, System Verilog various functional support, Partition Compile technology, parallel and distributed compilation, etc. To provide professional technical support for domestic and foreign first-class semiconductor design companies. During his tenure, he established and managed a number of research and development teams with a size of over 100 people. He has recruited and trained dozens of technical backbones from key universities domestic and overseas.

Title: Benchmark for VCD-Based FSM Coverage Statistics

Abstract: Coverage is an important indicator for measuring the quality of digital IC verification. Among them,

Finite State Machine Coverage (FSM Coverage) is an important component that measures the state and state transition coverage during the verification process. This talk will elaborate on the benchmark of X-EPIC's contest problem "VCD-Based FSM Coverage Statistics" in terms of setting evaluation indicators, selecting test cases, and building evaluation systems.

SPEAKER

Shuai Wu
Phlexing

Biography: Shuai Wu, an expert in Phlexing's product R&D, has more than 10 years' experience in RC and EMIR tools development. He has solid working experience with Fabs for projects of manufacturing chips with advanced nodes. He has profound knowledge-how about iterating with the advanced process odes.

Title: Machine Learning Driven Static IR Drop Estimation of SoC Power Grid Network

Abstract: In VLSI design, IR drop refers to the variation in electrical potential between the tow ends of a conducting wire when current flow through it. IR drop can happen in the power grid and ground network. As process technology keeps advancing and process nodes get ever smaller, the width between metal wires keeps shrinking, leading to ever increasing resistance per unit length. Thus, IR drop occurs in almost everywhere in the integrated circuits. The severe increase in IR drop could lead to malfunctioning of logic gates or even complete failure of instances and chips.

Phlexing's GloryBolt supports IC designs of tens-million instance and offers analysis results in power, IR drop, EM (electromigration) for singoff. GlroyBolt can allocate weakness of the power grid network in a fast manner. In a user-friendly manner, GloryBolt can quickly analyze data and summarize all data in proper format to allow users evaluate their chip designs and optimize to precision. This can accelerate design closure and signoff verification. The traditional analyzing method adopts KCL rule to calculate voltage values of millions of nodes. However, this method is rather time-consuming. Thus, we propose that the traditional method can be transformed into a machine learning (ML) method for predicting Static IR drop.

SPEAKER

Liwei Ni
Peng Cheng Laboratory

Biography: Liwei Ni received the M.Eng degree in Software Engineering at Beihang University, Beijing, China in 2021. Currently, he is pursuing Ph.D. degree in Computer Architecture at the Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, and is jointly trained with Pengcheng Laboratory. His research focues on the logic synthesis.

Title: Intelligent Flow for Logic Optimization and Technology Mapping

Abstract: Combination logic optimization and technology mapping are crucial processes in the front end of digital design. The netlist of combination logic undergoes simplification and remapping into equivalent netlists composed of logic units (LUTs) from the technology library, aiming to achieve optimized area and timing. Existing tools often employ fixed processes to complete optimization and mapping. This competition task requires an intelligent process to dynamically provide suitable optimization algorithm combinations based on the characteristics of the netlist. It should output a LUT (look-up table) netlist that is functionally equivalent, while optimizing the number of logic levels and LUTs.

The specified programming platform for the competition is iMap (https://gitee.com/oscc-project/iMAP). It has implemented basic algorithms such as rewrite, refactor, balance, and LUT mapping. Participants can design intelligent processes by combining these basic algorithms according to their algorithmic ideas and workload assessments (third-party tools and algorithms are not allowed). The iMap platform also supports parsing files in.aig format and outputting LUT netlists in .v format, enabling participants to focus on intelligent process design.

TUTORIAL

T06. Enabling Large Language Models in EDA

Chair: Bei Yu, The Chinese University of Hong Kong

Time	14:00-17:00 | May 10, 2024	Venue	2-6 / Baoji Hall

ABSTRACT

In this tutorial, we aim to showcase the transformative potential of large language models (LLMs) within the field of Electronic Design Automation (EDA). This session will explore a range of pioneering research efforts that leverage LLMs to address various EDA challenges, including "ChatEDA: A Large Language Model Powered Autonomous Agent for EDA," which introduces an LLM-powered tool for automating EDA tasks; "BetterV: Controlled Verilog Generation with Discriminative Guidance," focusing on generating more accurate Verilog code through LLMs; "SoLA: Solver-Layer Adaption of LLM for Better Logic Reasoning," which enhances LLMs' capability for logical reasoning in EDA applications. Participants will gain insights into the latest advancements in LLM applications for improving design automation, verification processes, and debugging efficiency, setting a new benchmark for innovation in EDA.

SPEAKER(S):

SPEAKER

Bei Yu

The Chinese University of Hong Kong

Biography: Prof. Bei Yu is currently an Associate Professor in the Department of Computer Science and Engineering, The Chinese University of Hong Kong. He has served as TPC Chair of ACM/IEEE Workshop on Machine Learning for CAD, and in many journal editorial boards and conference committees. He is Editor of the IEEE TCCPS Newsletter. He received ten Best Paper Awards from IEEE TSM 2022, DATE 2022, ICCAD 2021 & 2013, ASPDAC 2021 & 2012, ICTAI 2019, the VLSI Journal in 2018, ISPD 2017, SPIE Advanced Lithography Conference 2016, and six ICCAD/ISPD contest awards.

SPEAKER

Zhuolun He

The Chinese University of Hong Kong

Biography: Dr. Zhuolun He is currently a postdoctoral fellow at the Department of Computer Science and Engineering, Chinese University of Hong Kong, supervised by Prof. Bei Yu. He received his Ph.D. degree from CUHK in 2023, and his B.Sc. degree from Peking University in 2017. His research interests include LLM empowered EDA, efficient physical verification, and netlist representation learning.

SPEAKER

Hui-Ling Zhen

Huawei, Hong Kong

Biography: Dr. Hui-Ling Zhen is a principle research staff in Noah's Ark Lab, Huawei, Hong Kong. Before that, she is a post-doctoral research fellow in City University of Hong Kong, after she received the Ph.D degree in applied mathematics. Since joining Huawei, she has participated in the developments of mathematical programming solver, automatic test vector generation, logical equivalence testing, and model checking. She is also working on the research of next-generation EDA-tool enabled by LLM. Unitl now, she has published over 60 peer-reviewed papers in mainstream conferences and journals.

SPEAKER

Mingxuan Yuan
Huawei Noah's Ark Lab

Biography: Mingxuan Yuan received the Ph.D. degree in computer science from Hong Kong University of Science and Technology, China in 2011. He is currently a principal researcher of Huawei Noah's Ark Laboratory, China. His research interests include data-driven optimization algorithms, data-driven SAT/MIP solving algorithms and datadriven EDA algorithm.

TUTORIAL

T07. iEDA: An Open-source Physical Design EDA Infrastructure and Toolchain

Chair: Xingquan Li, Peng Cheng Laboratory

Time	14:00-17:00 | May 10, 2024	Venue	2-5 / Weinan Hall

ABSTRACT

By harnessing the capabilities of open-source software, the EDA tool provides an economical and adaptable solution suitable for designers, researchers, and enthusiasts alike. Open-source EDA fosters collaboration, innovation, and the exchange of knowledge within the EDA community. It underscores the pivotal role of the toolchain in expediting the development of electronic systems, while concurrently mitigating design expenses and enhancing design excellence. This tutorial centers on an open-source EDA infrastructure, iEDA, which is designed to establish a fundamental infrastructure for the evolution of EDA technology and bridge the gap between industry and academia in the EDA domain. To showcase the efficacy of iEDA, we have successfully fabricated and validated four chips of varying scales (ranging from 700k to 500M gates) using different process nodes (110nm and 28nm) with iEDA. iEDA is publicly accessible via the project's homepage at https://github.com/OSCC-Project/iEDA.

SPEAKER(S):

SPEAKER

Xingquan Li
Peng Cheng Laboratory

Biography: Xingquan Li is an associate researcher at Peng Cheng Laboratory (PCL). He received the Ph.D degree from Fuzhou University in 2018. His research interesting includes EDA and AI for EDA. His team has developed an open-source EDA infrastructure (iEDA). He has published over 40 papers in journals and conferences such as TCAD, TC, TVLSI, TODAES, DAC, ICCAD, DATE, ICCD, ASP-DAC, and has filed 13 invention patents. He has achieved first-place award from ICCAD@CAD Contest three times in 2017, 2018, and 2022. In 2020, he was honored with the Operational Research Application Award from the Chinese Operations Research Society. In 2023, he received the Best Paper Award from ISEDA.

SPEAKER

Zengrong Huang
Peng Cheng Laboratory

Biography: Zengrong Huang is an engineer at Peng Cheng Laboratory (PCL).

SPEAKER

Simin Tao
Peng Cheng Laboratory

Biography: Simin Tao is an engineer at Peng Cheng Laboratory (PCL).

SPEAKER

He Liu
Peking University
Biography: He Liu is a Ph.D student at Peking University.

SPEAKER

Shijian Chen
Peng Cheng Laboratory
Biography: Shijian Chen is a Ph.D student at Peng Cheng Laboratory (PCL).

SPEAKER

Weiguo Li
Minnan Normal University
Biography: Weiguo Li is a Master Student at Minnan Normal University.

SPEAKER

Zhisheng Zeng
Peng Cheng Laboratory
Biography: Zhisheng Zeng is a Ph.D student at Peng Cheng Laboratory (PCL).

TUTORIAL

T08. Introducing Building Blocks of DTCO

Host: Jinbin Deng, GWX Technology

Time	14:00-16:30 | May 10, 2024	Venue	2-1 / Xianyang Hall

ABSTRACT

For EDA vendors, DTCO (Design-Technology Co-Optimization) process enables wafer fabs and chip design companies to maintain close cooperation, reducing the development and usage risks of new semiconductor processes. OPC and Standard Cell Characterization are important building blocks in such flow. In LFD (Litho-Friendly Design) process, lithography hotspot pattern library is created at early-stage process nodes, which are then refined using previous models, machine learning, and OPC verification for accuracy. In practical design, pattern matching algorithms are employed to identify and correct hotspots within the design layouts (Hot-Spot Aware P&R). The established hotspot pattern library can be validated and optimized with real manufacturing data, ensuring its effectiveness for improved chip yield and manufacturability. Advanced device structures (such as FinFETs and GAA) cause self-heating issues, which further lead to problems with chip reliability (degradation). At the same time, chip design must ensure a zero-defect rate after manufacture and a longer operational lifespan, presenting significant challenges to chip design.

In this tutorial, GWX Library Characterization team introduces a highly accurate and efficient aging-aware stress analysis flow for CMOS circuits, incorporating a novel logical-resolving method and a machine learning-driven reliability analysis that significantly enhances STA efficiency and accuracy, guiding early-stage circuit design towards greater reliability. GWX Litho-team demonstrates a complete OPC flow and explains the concept of LFD in such process.

SMiXS team offers comprehensive chip design, verification, and mass production services, along with system-level package solutions and strategic partnerships, to enhance competitiveness and meet both Moore's Law and More-than-Moore demands, demonstrating success through advanced wafer processes and strong customer and supplier relationships.

SPEAKER(S):

SPEAKER

Lucas Lyu
GWX Technology

Biography: Lucas Lyu received the B.Eng. degree in electrical information engineering and the M.Eng. degree in computer engineering. His research interests include machine learning and applications in Library Characterization.

Title: Logical Resolving-Based Methodology and Machine Learning for Aging-Aware Library Characterization

Abstract: With rapid technology scaling of CMOS circuits, the performance degradation induced by the transistor aging is more evident, which leads to a more profound negative influence on the circuit. In this presentation, an accurate and efficient aging-aware stress analysis flow developed by the EsseChar team will be introduced, including a logical-resolving method of stress probability evaluation for aging and an accelerated reliability analysis approach based on machine learning. In the logical-resolving method, the aging dependence varying with workload changes is carefully considered for the first time. The accuracy is evaluated at the path level, guiding proper degradation path analysis and selection. Moreover, the technique captures the relationship between workload and aging delay with a minor error, lightening the over-pessimism of design margins for the aging-aware synthesis flow at the cell level. Additionally, a machine learning workflow has also been developed to enhance the efficiency of aging-aware library characterization. The experimental results demonstrate a symmetric mean absolute percentage error (SMAPE) of 0.6% for 562 delay timing arcs, and a 30% overall

speedup is expected in static timing analysis (STA) compared to simulation-based delay timing characterization. In conclusion, the accurate results from the proposed approach benefit the aging-aware STA flow, and a decent accuracy can be maintained while accelerating library characterization through the presented machine learning framework, hence providing constructive guidance in the early stage of circuit design for reliability.

SPEAKER

Lisa Wei
GWX Technology

Biography: Lisa Wei received her BS and MS in Chemistry. She had her first experience in semiconductor tape out at Semiconductor R&D center, Samsung Electronics. Since that she has been engaged in lithography modeling.

Title: OPC Introduction and Demonstration using EsseOPC (Part 1)

Abstract: Optical Proximity Correction (OPC) is a key process in semiconductor manufacturing, particularly in photolithography, which is the process of transferring a pattern onto a silicon wafer to create integrated circuits. As chip features become smaller and smaller due to advancements in technology, maintaining high resolution becomes challenging. OPC helps to enhance the resolution by compensating for distortions and imperfections that occur during the photolithography process. By improving pattern fidelity and minimizing defects, OPC contributes to higher chip yields during the manufacturing process. This is crucial for the economic viability of semiconductor fabrication. This speech will mainly introduce the basic process of OPC, as well as the main steps such as bias、dissection、retargeting、correction and verification. In addition, we plan to introduce an important concept for DTCO, the Litho-friendly Design (LFD), to the audience. We will demonstrate a complete OPC process example using the EsseOPC toolset by GWX Technologies during the class.

SPEAKER

Eric Pei
GWX Technology

Biography: Eric Pei received the B.E. degree in optical information of science and technology and the M.E. degree in optical engineering. He is experienced in rule-based and model-based OPC application.

Title: OPC Introduction and Demonstration using EsseOPC (Part 2)

Abstract: Optical Proximity Correction (OPC) is a key process in semiconductor manufacturing, particularly in photolithography, which is the process of transferring a pattern onto a silicon wafer to create integrated circuits. As chip features become smaller and smaller due to advancements in technology, maintaining high resolution becomes challenging. OPC helps to enhance the resolution by compensating for distortions and imperfections that occur during the photolithography process. By improving pattern fidelity and minimizing defects, OPC contributes to higher chip yields during the manufacturing process. This is crucial for the economic viability of semiconductor fabrication. This speech will mainly introduce the basic process of OPC, as well as the main steps such as bias、dissection、retargeting、correction and verification. In addition, we plan to introduce an important concept for DTCO, the Litho-friendly Design (LFD), to the audience. We will demonstrate a complete OPC process example using the EsseOPC toolset by GWX Technologies during the class.

SPEAKER

Grant Feng
SMIT XINXIN Semiconductor

Biography: Grant Feng holds a Ph.D degree. He has widely exposed to technology R&D, design ecosystem development, analog and digital IC design, supply chain management and business development.

Title: One-stop Chip Design, Verification and Production Service by SMiXS

Abstract: In response to the increasingly severe challenges imposed by Moore's Law and More-than-Moore, Shanghai SMIT XINXIN Semiconductor Co., LTD. (SMiXS) provides the one-stop chip design, verification, and mass production services to assist the academic research and empower the commercial products. In addition to the traditional System-on-Chip (SoC) design services to cover the digital design, Design-For-Testability (DFT) insertion, Intellectual Property (IP) customization, physical design and signoff, SMiXS also provides the system level package solution to address the More-than-Moore market demands. In order to help customers enhance their competitiveness in the fierce market competition, SMiXS has closely collaborated with its partners to create a reliable and competitive ecosystem in EDA/IP, wafer foundry, packaging and testing. Through in-depth collaboration with its customers, SMiXS has accomplished multiple successful cases on globally advanced wafer processes, packaging and testing platforms. All those successful cases not only demonstrated the core competency of SMiXS, also shown the persistent and resilient efforts of SMiXS to its commitment to achieve the win-win strategical relationship among SMiXS, its customers and its suppliers.

TUTORIAL

T09. Chip Verification Solution Based on Formal Verification

Time	14:00-14:45 | May 10, 2024	Venue	Network Security Bld. Room 713 Xidian University (South Campus)

ABSTRACT

Verification technology plays a pivotal role in ensuring the correctness of integrated circuit. Formal verification constitutes an integral component of verification technology. With the advanced technology development, formal verification is also experiencing growth and refinement. This presentation will conduct an in-depth exploration of multiple significant aspects of formal verification technology, including the development status of chip verification techniques, an introduction to formal verification methodologies, C/RTL-to-RTL equivalence checking,RTL/Netlist-to-Netlist equivalence checking, and model checking.

SPEAKER(S):

SPEAKER

Liva Ye

GWX Technology

Biography: Liva Ye, received her Bachelor of Engineering degree in Communication Engineering. She is currently immersed in the field of Electronic Design Automation (EDA) research and development. Her primary research areas are the development and application of formal verification tools.

TUTORIAL

T10. Application of Chip Verification Solutions

Time	14:00-17:00 | May 10, 2024	Venue	Network Security Bld. Room 708 Xidian University (South Campus)

ABSTRACT

This training course aims to provide an in-depth understanding of the core functionalities of S2C's digital EDA products and to analyze in detail the key challenges encountered in the chip design process and the corresponding strategies provided by EDA tools.

The course will use the "XiangShan" project from BOSC as an illustrative example, enabling participants to develop a systematic understanding of IC design verification processes and acquire comprehensive knowledge of prototyping analysis and practical skills. Additionally, the training will emphasize key points and practical challenges that are encountered during actual operations, helping participants establish a close connection between theoretical learning and practical application, effectively enhancing their practical abilities.

SPEAKER(S):

SPEAKER

Cindy Liang
S2C

Biography: Cindy Liang has 8 years of hardware design and 5 years of architecture simulation experience in the semiconductor industry. She graduated from Northwestern Polytechnical University with a bachelor's degree and a master's degree from Xi'an Institute of Microelectronics Technology in computer architecture.

TUTORIAL

T11. Training and Demonstration of EDA Tools for the Full Process of RF Circuit Design

Time	14:00-16:00 | May 10, 2024	Venue	Network Security Bld. Room 709 Xidian University (South Campus)

ABSTRACT

This training is based on Empyrean's full process EDA tool for RF circuit design. It provides a detailed introduction to Empyrean Technology and its full process products, helping everyone understand Empyrean's tools and design process. This includes RF model extraction tool, RF circuit schematic editing tool, RF circuit layout editing tool, RF circuit simulation tool, RF circuit physical verification tool, etc., providing users with a complete solution from circuit to layout, from design to simulation verification.

SPEAKER(S):

SPEAKER

Han Yu

Empyrean Technology

Biography: Marketing Cooperation Director of Empyrean Technology, with the Chinese National Senior Engineer Title, graduated from Beihang University with Master Degree in 2007. He worked for Empyrean Technology Corp. (Empyrean) from 2010 till now.

He is now the Senior Technical Marketing Director of Empyrean, leading some business including external technical corporation and university programs.

He has published over 10 articles on academic journals such as IEEE-DAC, ACM-GLSVLSI, China Integrated Circuit etc. as the first author. He has also served as a review expert of the "National Project of Micro-Nano Electronics", the deputy director of the editorial board of "National Vocational and Technical Skill Standards - Integrated Circuit Engineering", and the director of Guangdong EDA Engineering Center.

TUTORIAL

T12. Design Enablement Solution for Novel Semiconductor Devices Research

Chair: Qin Chao Zheng, Primarius

Time	14:00-17:00 | May 10, 2024	Venue	Network Security Bld. Room 707 Xidian University (South Campus)

ABSTRACT

The advancement in semiconductor research has led to the development of novel devices and materials with superior performance. Integrating these innovations into existing chip design flow is essential, requiring the creation of SPICE models, Process Design Kits (PDKs).

The development of SPICE models and PDKs for novel devices places high demands on the flexibility and scalability of EDA tool. Primarius's EDA products address these requirements comprehensively, offering robust support for these tasks.

This tutorial, "Design Enablement Solution for Novel Semiconductor Devices Research," focuses on novel semiconductor devices such as wide bandgap semiconductors (SiC, GaN etc.), Thin-Film Transistors (TFT), and superconducting Josephson junctions. It offers unique hands-on experimental opportunities for participants to directly engage with these technologies using Primarius's tools.

This session will enable attendees to understand and apply the methodologies necessary for incorporating high-performance novel devices into mainstream chip designs. Join us to explore essential techniques in novel devices design enablement and transition pioneering research into practical applications.

SPEAKER(S):

SPEAKER

Chen Le Le
Primarius

Biography: R&D Senior Director, graduated from the Shanghai Institute of Microsystem and Information Technology at the Chinese Academy of Sciences, earning a Ph.D. in Microelectronics and Solid State Electronics. Previously worked at HHGrace and SMIC, where he was involved in the development of 0.18um SiGe HBT BiCMOS process technology, 28nm HKMG process technology, and advanced FinFET process technology. As the first author, he has published 4 technical articles in domestic and international journals and conferences and holds over 20 patents, including one U.S. patent.

SPEAKER

Qin Chao Zheng
Primarius

Biography: Senior Manager in the New Solution Department, holding a Master's degree in Electromobility Engineering from Chemnitz University of Technology, Germany. Mentored by Professor Josef Lutz, a renowned power semiconductor expert, with specialization in IGBT device modeling, simulation, and testing. Currently focusing on the development and integration of third-generation semiconductor solutions.

PANEL

P1. 2.5D/3D Heterogeneous Integration: Challenges and Opportunities

Time	13:30-15:30 | May 11, 2024	Venue	2-6 / Baoji Hall

ABSTRACT

With the continuous shrinking of chip feature size, the continuation of Moore's Law becomes an increasingly challenging task. The emerging of AI and cloud computing aggravates the problem further. 2.5D Chiplet and 3D stacking for heterogeneous integration becomes one of promising technologies to build "Big Chips", which can provide ultra-high bandwidth and computing efficiency within acceptable budget. This panel invites some experts working in this field to introduce their pioneering work in 2.5D/3D integration and share their viewpoints of the prospects of 2.5D/3D integration. This event is partially supported by IEEE CEDA Beijing Chapter.

Session Organization and Speakers:

Session Chair/Moderator

Yuanqing Cheng
Beihang University

Panelists

Each panelist can prepare a 10-15min talk to present his/her ideas and insights at the beginning of the panel session, and later defend during the panel discussion.

"For" Group Speaker

Ying Wang
Institute of Computing Technology, Chinese Academy of Sciences

Biography: Dr. Ying Wang is a professor in Institute of Computing Technology, Chinese Academy of Sciences, Beijing, and his current research interest includes the chip design automation, reliable computer architecture and memory system. He has published over 100 papers on IEEE/ACM conferences and journals, including TC, DAC and ICCAD. He has received several awards from international conferences, including the championship of IEEE LPIRC contest at DAC 2016, the championship of the System Design Contest at DAC 2018, the Best Paper Award at ITC-Asia and ICCD.

Title: A 22nm 1024-core RISC-V Processor Agile Customized by 64 Reusable Chiplets with Low-latency High-flexibility Die-to-Die Interconnection

Abstract: Designing a customized many-core processor typically takes considerable efforts and time overhead, leading to a significant gap between evolving application requirements and lengthy design cycles. In recent years, chiplet-based integration emerges as an agile solution by reusing pre-fabricated dies. We design a chiplet (Zhejiang-1) featuring low-latency, flexible die-to-die interconnects, supporting various inter-core topologies. Additionally, we propose the Sunflower architecture for chiplet integration with advanced packaging. Finally, we employ the proposed chiplets to customize 1024-core processors for privacy computing and neuromorphic computing as a test-case of agile chiplet-based design flow.

"For" Group Speaker

Qinzhi Xu

Institute of Microelectronics, Chinese Academy of Sciences

Biography: Doctor Qinzhi Xu is currently a professor and doctoral supervisor in Institute of Microelectronics of the Chinese Academy of Sciences. His main research interests focus on multiphysics modeling and software development of heterogeneous integration systems, theories and modeling simulators of chemical mechanical planarization, design for manufacturability in nano-scale integrated circuits and development of models and simulation tools for predicting the structure and properties of polymeric materials. He has undertaken more than 20 National, Beijing City, Chinese Academy of Sciences and Enterprise projects, published over 40 modeling papers in interdisciplinary fields of integrated circuits, EDA, polymer nanocomposites, and computational chemistry as the first or corresponding author, applied for nearly 50 patents as the first inventor and obtained several software copyrights of chiplet simulation. He also has received the Third Prize of Beijing Science and Technology Award and the Second Prize of Science and Technology Award of the Chinese Institute of Electronics.

Title: Multiphysics Simulation of Chiplet Heterogeneous Integration System

Abstract: Entering the post Moore era, silicon based CMOS technology faces significant challenges in terms of physical principles and process technologies by reducing size to improve integration. The manufacture cost and design difficulty of system on a chip (SoC) technology gradually increase in recent years. Chiplet heterogeneous integration (CHI) technology, which can divide the large SoC chip into small ones, becomes an important technology because of its reduction of manufacture cost and improvement of chip yield. However, the increase of power density and the deterioration of heat dissipation environment strongly influence the functionality and stability of chips and integrated systems. The coupling effect of electrical, thermal, and mechanical stress poses a serious challenge to the reliability of CHI system. Therefore, the multiphysics simulation of CHI system has become a key technology that urgently needs to be solved in the EDA industry. This talk will briefly introduce the research background, technical challenges, and research progress of CHI systems. Some suggestions for multiphysics simulation of CHI systems will also be provided.

"Against" Group Speaker

Xiangkun Yin

Xidian University

Biography: Xiangkun Yin, received the Ph.D. degree from School of Microelectronics, Xidian University in 2017. From 2019 to 2020, he conducted academic research as a visiting scholar with the School of Computer Science, University of Manchester, United Kingdom. And now, he is Associate professor with the School of Integrated Circuits, Xidian University. His current research interests including 3-D ICs based on the TSV, and silicon-based RF/Microwave circuits and Micro-systems. He has authored over 30 internationally refereed journal articles and more than 20 international conference papers. He is also a reviewer of the IEEE Transactions on Microwave Theory and Techniques, the IEEE Microwave and Wireless Technology Letters, the IEEE Transactions on Electromagnetic Compatibility.

Title: Research Progress of Silicon-based 3D Integrated Passive Devices and Circuits with Through-Silicon Vias Technology

Abstract: For more than half a century, integrated circuit has consistently followed Moore's Law in scaling down the technology node. As the future Moore's Law is reaching limitation, the continuous needs for increased performance, further miniaturization and reduced cost have driven the development of new and more advanced integrating and innovation packaging solutions. The emerging three-dimensional integrated circuit (3-D IC) technology, stacking multiple silicon layers vertically, offers an attracting solution to footprint miniaturization and monolithic integration of multiple modules and integrated passive devices. However, some critical challenges remain in the high-density interconnections and high-quality passive components. On the one hand, with the improvement of the system functions and complexity, the signal interconnection density among multiple modules are dramatically increased, which introduces serious problems such as electromagnetic loss,

transmission delay, signal distortion, and dramatic increase in power consumption. On the other hand, limited by the dielectric constant and magnetic permeability of semiconductor materials, the capacitance density and inductance density of passive components are difficult to be significantly improved within the existing framework and technology, resulting in key passive components such as capacitors, inductors, filters, etc., which always consume a large footprint. In this work, some of the latest research progress of broadband interconnect structures and integrated passive devices and circuits based on silicon-based 3D integration technology and Through-silicon via (TSV) is introduced, and the development trends of various devices and functional circuit modules are prospected and discussed.

"Against" Group Speaker

Yang Yu

Harbin Institute of Technology

Biography: Yang Yu (Senior Member, IEEE) received her B.S., M.S. and Ph.D. degrees with the Department of Automatic Test and Control from the Harbin Institute of Technology in Harbin, China in 2002, 2004 and 2008, respectively.

She is currently a Full Professor with the Department of Test and Control Engineering, School of Electronics and Information Engineering, HIT. Shi is also the Deputy Dean of School of Future Technology, HIT, China. Her current research interests include automatic testing, diagnostic and prognostics for electronics and electrical systems. She is the Vice President of IEEE WIE(Harbin).

Title: Key Test Techniques for M3D ICs

Abstract: Monolithic three-dimensional integrated circuits (M3D ICs) have higher integration and better performance compared to 3D ICs based on through-silicon vias (TSVs). However, high integration density and substantial scaling of the inter-layer dielectric (ILD) make M3D ICs extremely prone to process defects. M3D IC testing is essential to ensure the large-scale application of M3D ICs. This report will share the opportunities and challenges faced by M3D integration technology, and introduce existing M3D IC test technologies. Furthermore, we will introduce the relevant work carried out by our team, including ILD void detection technology and MIV test technology. The proposed works have high test resolution while ensuring low test overhead.

PANEL

P2. LLM for Chip Design: Challenge and Opportunities

Time	16:00-18:00 | May 12, 2024	Venue	2-6 / Baoji Hall

ABSTRACT

Recently, the rapid progress of large language models (LLM) has brought new opportunities and possibilities to automatic hardware design fields. This panel aims to bring together the pioneers who have either research experience or practiced this new design paradigm in their works, and share their valuable views and first-hand conclusions about the exploration of LLMs in the area of EDA and architecture design. The topic to be covered includes how to utilize the interactive LLMs to accelerate chip design (Both logic level and physical level), synthesis and verification processes, and how to finally achieve zero-code EDA innovation by means of AI agents. We will bring together researchers, industry experts to exchange ideas, share experiences, and discuss the latest advancements in LLM for EDA methodologies, algorithms, and tools.

KEY QUESTIONS

Question 1: Do you think LLM or AI will replace some of the tools in the EDA flow? Do you think it will eventually change the whole process and achieve end-to-end silicon compilation?

Question 2: Can LLM help EDA tool to achieve no-human-in-the-loop design process, or become an easy-to-use interface that better interact with designs as a pilot? What's the most significant challenges and opportunities in end-to-end chip design agent?

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Session Organization and Speakers:

Session Chair/Moderator

Ying Wang
Institute of Computing Technology, Chinese Academy of Sciences

Panelists

Each panelist can prepare a 10-15min talk to present his/her ideas and insights at the beginning of the panel session, and later defend during the panel discussion.

"For" Group Speaker

Zidong Du
Institute of Computing Technology, Chinese Academy of Sciences

Biography: Zidong Du is an associate professor at Intelligent Processor Research Center, Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS). His research interests mainly focus on novel architecture for artificial intelligence, including deep learning processors, inexact/approximate computing, neural network architecture, neuromorphic architecture. He has published over 20 top-tier computer architecture research papers, including ASPLOS, MICRO, ISCA, TC, TOCS, TCAD. For his innovative works on deep learning processors, he won the best paper award of ASPLOS'14, Distinguished Doctoral Dissertation Award of CAS (40/10000), Distinguished Doctoral Dissertation Award of China Computer Federation (10 per year).

"For" Group Speaker

Junchi Yan
Shanghai Jiao Tong University

Biography: Junchi Yan, Full Professor in Department of Computer Science & Engineering, Shanghai Jiao Tong University. He is the PI of many major projects of the Ministry of Science and Technology/NSFC/Ministry of Education. He was once the chief researcher of cognitive computing with IBM China Research. He has published over 200 CCF-A papers as first/correspondence authors, and the google scholar citation is approaching 17000. He is a Fellow of IET.

"For" Group Speaker

Xi Wang
Southeast University

Biography: Xi Wang is a professor in Southeast University, Nanjing. He received the Ph.D. degree in computer science from Texas Tech University, Lubbock, TX, USA, in 2020, under the advisement of Dr. Yong Chen and Dr. John D. Leidel. He is a also Senior Engineer with the National Center of Technology Innovation for EDA, Nanjing, China. He was the Post-Doctoral Researcher and a Research Scientist with the RIOS Laboratory, Tsinghua University, Beijing, China, working under the guidance of Dr. David A. Patterson and Dr. Zhangxi Tan. His research interests include computer architectures, agile hardware design, EDA, compilers, machine learning, and parallel computing. (Based on document published on 20 December 2023).

"Against" Group Speaker

Qiang Xu
The Chinese University of Hong Kong

Biography: Qiang Xu is a Professor at The Chinese University of Hong Kong, his current research interests are in the broad areas of AI and EDA. He has published 180+ papers with 8000+ citations, including several best papers at prestigious conferences and an ICCAD Ten Year Retrospective Most Influential Paper. He has supervised ~20 Ph.D. dissertations and his students have won EDAA Outstanding Dissertation Award and the semi-finals of IEEE TTTC Doctoral Thesis Award.

"Against" Group Speaker

Bei Yu
The Chinese University of Hong Kong

Biography: Bei Yu is currently an Associate Professor at the Department of Computer Science and Engineering, The Chinese University of Hong Kong. He received PhD degree from Electrical and Computer Engineering, the University of Texas at Austin in 2014. His current research interests include machine learning with applications in VLSI CAD and computer vision. He has served as TPC Chair of 1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), served in the program committees of DAC, ICCAD, DATE, ASPDAC, ISPD, the editorial boards of ACM Transactions on Design Automation of Electronic Systems (TODAES), Integration, the VLSI Journal. He is Editor of the IEEE TCCPS Newsletter. Prof. Yu received seven Best Paper Awards from ASPDAC 2021 & 2012, ICTAI 2019, Integration, the VLSI Journal in 2018, ISPD 2017, SPIE Advanced Lithography Conference 2016, ICCAD 2013, six other Best Paper Award Nominations (DATE 2021, ICCAD 2020, ASPDAC 2019, DAC 2014, ASPDAC 2013, and ICCAD 2011), six ICCAD/ISPD contest awards.

"Against" Group Speaker

Jianwang Zhai
Beijing University of Posts and Telecommunications

Biography: Jianwang Zhai is currently an assistant professor at Beijing University of Posts and Telecommunications (BUPT). Prior to that, he got his Ph.D. in Computer Science and Technology from Tsinghua University (THU) in 2023, and received my B.Eng. from Beijing Jiaotong University (BJTU) in 2018. My research interests include machine learning and optimization methods with applications in EDA, especially power modeling, design space exploration, and physical design.

PANEL

P3. The Future of Analog CAD: Navigating the Spectrum between Full Automation and Human Expertise

Time	16:00-18:00 | May 12, 2024	Venue	2-5 / Weinan Hall

ABSTRACT

In recent years, the field of analog integrated circuit (IC) design has been transformed by significant advances in design automation. Initiatives like DARPA's "no-human-in-the-loop" programs and subsequent research projects have pushed the boundaries of fully-automated Electronic Design Automation (EDA) software, aiming to revolutionize the industry's traditional workflows. However, alongside these advancements, there's a growing body of research advocating for the retention of human involvement, particularly through approaches like interactive analog layout design. This panel seeks to explore the evolving role of humans in analog CAD, debating the merits and demerits of full automation versus human-in-the-loop approaches. It will convene experts from academia, engineering, and business to provide a comprehensive perspective on this critical junction in CAD technology's future. The discussion aims to unravel whether the pursuit of complete automation is the ideal path or if the nuanced judgment of human engineers still holds indispensable value in the analog design process.

KEY QUESTIONS

Question 1: Integration and Performance: How can current automated EDA tools for analog IC design be effectively integrated into existing design flows, and what are their performance benchmarks compared to traditional methodologies?

Question 2: Human-Tool Interaction: In what specific areas of analog IC design does human expertise significantly outperform automated systems, and how can these areas be optimally integrated with automated processes?

Question 3: Future Directions in Analog CAD: Considering current trends and technological capabilities, should the industry focus more on advancing towards fully-automated analog CAD tools, or should there be a strategic shift towards enhancing human-computer collaboration? What are the technical and practical considerations that should guide this decision?

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Session Organization and Speakers:

Session Chair/Moderator

Keren Zhu
The Chinese University of Hong Kong

Panelists

Each panelist can prepare a 10-15min talk to present his/her ideas and insights at the beginning of the panel session, and later defend during the panel discussion.

"For" Group Speaker

Xuan Zeng (Online)

Fudan University

Biography: Xuan Zeng received the B.S. and Ph.D. degrees in electrical engineering from Fudan University, Shanghai, China, in 1991 and 1997, respectively., She is currently a Full Professor with the Microelectronics Department, Fudan University, where she served as the Director of the State Key Laboratory of Application Specific Integrated Circuits and Systems from 2008 to 2012. She was a Visiting Professor with the Department of Electrical Engineering, Texas A&M University, College Station, TX, USA, and the Microelectronics Department, Technische Universiteit Delft, Delft, The Netherlands, in 2002 and 2003, respectively. Her current research interests include analog circuit modeling and synthesis, design for manufacturability, high-speed interconnect analysis and optimization, and circuit simulation., Prof. Zeng received the Changjiang Distinguished Professor with the Ministry of Education Department of China in 2014, the Chinese National Science Funds for Distinguished Young Scientists in 2011, the First-Class of Natural Science Prize of Shanghai in 2012, the 10th For Women in Science Award in China in 2013, and the Shanghai Municipal Natural Science Peony Award in 2014. She received the Best Paper Award from the 8th IEEE Annual Ubiquitous Computing, Electronics and Mobile Communication Conference 2017. She is an Associate Editor of IEEE Transactions on Circuits and Systems—Part II: Express Briefs, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, and ACM Transactions on Design Automation of Electronic Systems.

"For" Group Speaker

Zhou JIN

China University of Petroleum, Beijing

Biography: Dr. Zhou JIN received her M.S. and Ph.D. degrees from the Graduate School of Information, Production, and Systems at Waseda University in Japan in 2012 and 2015, and B.S. degree from Nanjing University in 2010. Currently, she is as an Associate Professor with the Super Scientific Software Lab at China University of Petroleum-Beijing. Her research interests mainly focus on simulation and verification technologies for nonlinear large-scale integration (LSI) circuits and systems, AI and GPU acceleration in Electronic Design Automation (EDA), and parallel linear algebra. She actively leads or takes part in multiple government-funded and industrial collaborative projects, such as the National Science Foundation of China's Key Programs, China's National Key R&D Program, and Programs from leading industries. Her work has been extensively published at top-tier conferences and journals, including DAC, TCAD, PPoPP, IPDPS, and TODAES. She was a recipient of IEEJ Kyushu Branch Chairman's Award and Young Elite Scientists Sponsorship Program of Beijing Association for Science and Technology.

"For" Group Speaker

Yang Liu

Empyrean Technology Co.

Biography: Yang Liu is a senior product director at Empyrean Technology Co. He obtained his Ph.D. from Tsinghua University and has twenty years of experience in the EDA (Electronic Design Automation) industry. His research interests include circuit simulation and high-performance computing among other areas.

"Against" Group Speaker

Guoyong Shi

Shanghai Jiao Tong University

Biography: Guoyong Shi is currently a full professor of the School of Microelectronics, Shanghai Jiao Tong University. He received the Bachelor of Science degree in Applied Mathematics from Fudan University, Shanghai, China in 1987, the Master of Science degree in Electronics and Information Science from Kyoto Institute of Technology, Kyoto, Japan in 1997, and the Ph.D. degree in Electrical Engineering from Washington State University, Pullman, USA in 2002. He visited Eindhoven University of Technology as a visiting research fellow from January to June 2001. From August 2002 to June 2005, he was a postdoctoral research fellow in the Department of Electrical Engineering, University of Washington in Seattle, USA, working on Electronic Design Automation. His current research interests include design automation tools for nanometer integrated circuits, with focuses on symbolic simulators, variation-aware signal analysis and statistics tools, and future-technology oriented design automation tools. He has published about 40 research papers in the areas including Computer-Aided VLSI Design and Control Theory.

"Against" Group Speaker

Zuochang Ye

Tsinghua University

Biography: Zuochang Ye received the B.S. and Ph.D. degrees from Tsinghua University, Beijing, China, in 2002 and 2007, respectively., From 2007 to 2008, he was a Research Scientist with the Cadence Research Laboratories, Berkeley. He is currently an Associate Professor with the Institute of Microelectronics, Tsinghua University. His research interest is computer-aided design for VLSI circuits, particularly on numerical algorithms for EM simulation and circuit simulation.

"Against" Group Speaker

Xiyuan Tang

Peking University

Biography: Xiyuan Tang is currently an assistant professor at Peking Unversity. Xiyuan received the B.Sc. degree (Hons.) from the School of Microelectronics, Shanghai Jiao Tong University, Shanghai, China, in 2012, and the M.S. and Ph.D. degree in electrical engineering from The University of Texas at Austin, Austin, TX, USA, in 2014 and 2019 respectively. From 2014 to 2017, he was a Design Engineer with Silicon Laboratories, Austin, TX, where he was involved in the RF receiver design. He was a postdoctoral researcher at University of Texas at Austin from 2019 to 2021. His current research interests include analog/mixed-signal circuits, intelligent sensors, and ICs for human healthcare.

PANEL

P4. When Math Meets EDA: A Tale of Two Disciplines

Time	16:00-18:00 | May 12, 2024	Venue	2-1 / Xianyang Hall

ABSTRACT

It turns out that the EDA industry is already full of math and advanced numerical computation. In this panel session, a few topics on the interdisciplinary research on mathematics and EDA will be discussed and debated by the panelists.

KEY QUESTIONS

Question 1: Why is the interdisciplinary research on mathematics and EDA important?

Question 2: What are the challenges of interdisciplinary collaborations between mathematician and microelectronic scientist?

Question 3: Who will play a prominent role in the interdisciplinary research? mathematician? or microelectronic scientist?

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Session Organization and Speakers:

Session Chair/Moderator

Tao Cui
Academy of Mathematics and Systems Science, CAS

Panelists

Each panelist can prepare a 10-15min talk to present his/her ideas and insights at the beginning of the panel session, and later defend during the panel discussion.

"For" Group Speaker

Yangfeng Su
Fudan University

Biography: Yangfeng Su received the B.S. and Ph.D. degrees in computational mathematics from Fudan University in 1986 and 1992, respectively. He is a Full Professor with the School of Mathematical Sciences, Fudan University. His research interest is numerical linear algebra, with emphasis on the applications in electronic design automation.

"For" Group Speaker

Wenxing Zhu
Fuzhou University

Biography: Wenxing Zhu received his B.S. degree in Mathematics, and M.S. and Ph.D. degrees in Operations Research, all from Shanghai University in 1989, 1992, and 1996, respectively. He is a "Jiaxi" Distinguished Professor at the Center for Discrete Mathematics and Theoretical Computer Science, Fuzhou University. His main research interest lies in VLSI Physical Design and Discrete Optimization.

His research was mainly supported by the National Natural Science Foundation of China and the National Key Research and Development Program of China. He has published more than 100 papers in reputed academic journals and conferences, such as IEEE TCAD, IEEE TC, DAC, ICCAD, and INFORMS JOC, etc. He was awarded the First Prize of Natural Sciences by the Ministry of Education of China in 2022; and the Application Award of Operations Research by the Operations Research Society of China in 2020. He received the Best Paper Awards from DAC 2017 and ISEDA 2023, and was nominated for the Best Paper Award at ICCAD 2018 and CCF-DAC 2023. He also received the Second Prize for National Teaching Achievement in 2009.

"For" Group Speaker

Yingzhou Li
Fudan University

Biography: Yingzhou Li is an Assistant Professor at Fudan University. Li obtained his Ph.D. from Stanford University in 2017 and was a Phillip Griffiths Research Assistant Professor at Duke University from 2017 to 2020. His research focuses on designing and analyzing efficient algorithms to address problems from various fields, including differential and integral equations, computational chemistry, machine learning, quantum computing and EDA.

"Against" Group Speaker

Quan Chen
Southern University of Science and Technology

Biography: Quan Chen graduated from the Department of Electrical and Electronic Engineering at the University of Hong Kong. He was then a postdoctoral fellow at the University of California, San Diego (UCSD) and a research assistant professor at the University of Hong Kong. In 2019, he joined the School of Microelectronics, Southern University of Science and Technology as an assistant professor. Dr. Chen focuses on large-scale analog/RF circuit simulation, multiphysics analysis, and TCAD simulation of advanced semiconductor devices in electronic design automation (EDA). He has received the 2012 ICCAD Best Paper Award Nomination and the second prize of the 2020 Wu Wenjun Artificial Intelligence Chip Award, and was selected for the Shenzhen Peacock Team. He is leading or participating in multiple government-funded projects, including the Key and the Special Programs of NSFC and the Key R&D Program of Guangdong Province, as well as several industrial collaborative projects. He has rich experience in EDA technology transfer and commercialization.

"Against" Group Speaker

Lang Zeng
Beihang University

Biography: Lang Zeng studied at the School of Electronics Engineering and Computer Science of Peking University in 2003 and received B.S. degree in 2007. Entered the Institute of Microelectronics Peking University in the same year, went on study exchange program at Purdue University from 2009 to 2011 and received PhD degree in 2012. His doctoral dissertation titled, "Research on the Characteristics of New Semiconductor Devices and Fast Algorithm of Quantum Transport" won the Excellent PhD Dissertation of Peking University. Continued his postdoctoral research and was awarded the title of Outstanding Postdoctoral Fellow by Peking University. In 2014, Prof. Zeng joined the Center for Spintronics Interdisciplinary Research at Beihang University, with research interests in quantum transport in nanoscale transistors and spin transport in two-dimensional materials and Magnetic Tunneling Junctions.

FORUM

EDA Contest

Chair: Bo Jiang, Nanjing University of Posts and Telecommunications

Time	13:30-17:00 | May 11, 2024	Venue	3-6 / Yulin Hall

TAIK DETAILS

13:30-13:50 | Fangzhou Liu, The Chinese University of Hong Kong

Speech Title: BETuning: Intelligent Synthesis Recipe Search Strategy Based on Multi-Armed Bandit and Evolutionary Algorithms

Bio: Fangzhou Liu is currently a Ph.D. student in the Department of Computer Science and Engineering at The Chinese University of Hong Kong, under the supervision of Prof. Bei Yu. Previously, she received her B.E. from the School of Electronic Science and Engineering at Nanjing University. She and her team won the Qilin Cup at the 5th Integrated Circuit EDA Design Elite Challenge.

Abstract: In logic synthesis, the optimization of combinational logic is a crucial step. A common approach in many open-source tools involves applying a series of optimization transformations to Boolean networks, such as And-Inverter Graphs (AIG). These transformations include rewriting, refactoring, and balancing, with the aim of simplifying and enhancing the network structure to reduce circuit area and delay. Given that the process of finding an optimal sequence of operations is a complex exploration task in design space with an exponential solution space, finding an efficient method is particularly important. In our research, we employed a strategy that combines Multi-Armed Bandit (MAB) algorithms with Evolutionary Algorithms (EA). This combination allowed the algorithm to perform searches ranging from fine-grained to coarse-grained within a limited timeframe, extending the optimization sequence as much as possible and achieving significant optimization results.

13:50-14:10 | Zhengzhe Zheng, Southeast University

Speech Title: Automatic Standard Cell Layout Synthesis

Bio: Zhengzhe Zheng, received his Bachelor's degree in Electronic Science and Technology from Southeast University in 2022. He is currently pursuing the Master's degree at school of Integrated Circuits, Southeast University. He received the first place in Topic 8 of the 5th Integrated Circuit EDA Design Elite Challenge.

Abstract: Standard cells are essential components of modern digital circuit designs, and therefore, the layout generation of standard cells is crucial in today's VLSI design flow. We propose a standard cell circuit synthesizer that utilizes an SMT solver with multiple optimization objectives for transistor placement. In addition to transistor placement rules, we have incorporated constraints and optimization objectives within the SMT solver to enhance the routability of the layout results.

14:10-14:30 | Kai Jing, Southeast University

Speech Title: Efficient and Accurate Implementation of Statistical Static Timing Analysis Algorithm

Bio: Kai Jing received his B.E. degree from the School of Electronic and Information Engineering at Soochow University in 2022. Currently, he is pursuing his M.E. degree at the School of Integrated Circuits, Southeast University. His research interests include static timing analysis and statistical timing characterization methodologies. He was awarded the Elite Cup in the 5th Integrated Circuit EDA Elite Challenge in 2023.

Abstract: Static timing analysis is a vital stage in digital integrated circuit design from logic synthesis to physical implementation. We propose an efficient and precise implementation for statistical static timing analysis (SSTA) owing to the customized depth-first search algorithm and global path-first distributed propagation method, which guarantee the precision of endpoint slack and global slack computations. Moreover, we employ techniques including name mapping functions and file preprocessing, which achieves significant runtime speedup and memory consumption reduction.

14:30-14:50 | Yujiao Deng, Southwest Jiaotong University

Speech Title: Fast Layout Pattern Matching based on DFA

Bio: Yujiao Deng is a postgraduate at the School of Information Science and Technology, Southwest Jiaotong University. Her research focuses on the AI prediction model for timing. In the EDA Elite Challenge Contest@2023, she won the TOP3 Cup of the contest and rank 1st of the pattern matching problem.

Abstract: As chip manufacturing processes approach physical limits, the probability of defects in chips after photolithography increases significantly due to specific patterns in the chip layout, whitch called photolithography hotspots. To improve chip yield, we need a method to identify hotspots in the layout for subsequent correction. To this end, we propose a method that accelerates layout template matching using Deterministic Finite Automata (DFA). Our approach transforms the polygon matching problem into a string matching problem and accelerates it using DFA, achieving high parallelism for precise layout pattern matching.

14:50-15:10 | Yilu Chen, Fuzhou University

Speech Title: Machine Learning Driven Static IR Drop Estimation of SoC Power Grid Network

Bio: Yilu Chen received the B.S. degree and M.S. degree from Fuzhou University, Fuzhou, China, in 2018 and 2021, respectively, and he is a Ph.D. candidate in the College of Mathematics and Statistics at Fuzhou University. He was recipients of the Second Place in the ICCAD 2023 CAD Contest and two first prizes of the Integrated Circuit EDA Elite Challenge. His current research interests include logic synthesis, physical design, machine learning and machine learning in EDA.

Abstract: Static IR drop analysis is a fundamental and critical task in chip design since the IR drop will significantly affect the design's functionality, performance, and reliability. However, the process of IR drop analysis can be time-consuming, potentially taking several hours. In this talk, we introduce a Transformer-based Inception U-Net for static IR drop estimation. In addition, we propose an MLP model to further optimize the final performance.

15:10-15:30 | Mingjun Wang, Gu Feng, Institute of Computing Technology

Speech Title: Accelerating Fault Simulation on ARM Multi-core CPUs: Innovations and Optimizations

Bio: Wang Mingjun and Gu Feng both received their B.S. degrees from Peking University and are now pursuing their Master's degrees at the University of Chinese Academy of Sciences. They are engaged in research at the State Key Lab of Processors and are key researchers at CASTEST Co., Ltd. Their focus is on the design for testability and functional safety in electronic systems, particularly exploring innovations in fault simulation on ARM multi-core CPU architecture. Their research has garnered recognition, including first place in the prestigious Xiakedao contest.

Abstract: Fault simulation is crucial in the design for testability (DFT) processes, including automatic test pattern generation (ATPG) and fault diagnosis, to ensure the reliability of electronic systems. The challenge lies in accelerating these simulations effectively on multi-core systems. Our team proposes a transformative approach leveraging the ARM multi-core CPUs which significantly enhances fault simulation efficiency. We address both the logical complexity and memory access bottlenecks typical in these simulations. Through optimizing memory usage and exploiting parallel processing capabilities of ARM CPUs, we have substantially improved the simulation speed. Our method demonstrates outstanding performance, scalability, and efficient memory utilization across various benchmark circuits, validating the effectiveness of our approach in streamlining electronic design automation (EDA).

This presentation outlines our work on developing a scalable parallel fault simulator that efficiently utilizes the architectural characteristics of ARM multi-core CPUs, providing a cornerstone for future advancements in the field of fault simulation.

15:30-16:00 | Break

16:00-16:20 | Jiechen Huang, Tsinghua University

Speech Title: A Complex Symmetric Linear Solver Towards Power Grid Analysis in Xiakedao Contest

Bio: Jiechen Huang is a second-year Ph.D. student at Tsinghua University, advised by Prof. Wenjian Yu. He received the B.S. in computer science from Tsinghua University in 2022. His research interests include numerical computing and capacitance extraction.

Abstract: One of Xiakedao Contest Problems focuses on power gird analysis, requiring solution of sparse linear systems. In the context of frequency domain analysis, the coefficient matrix is complex and symmetric, but not necessarily positive definite. We develop an efficient linear solver towards this contest that uses the Bi-CGSTAB and LDL decomposition algorithms. With high speed and low memory footprint, our solver won first place in the

contest.

16:20-16:40 | Shuo Yin, The Chinese University of Hong Kong

Speech Title: ODC Computation for Clock Gating

Bio: Shuo Yin received his B.S. degree from Beihang University in 2022. He is currently a second-year Ph.D. student in the Department of Computer Science and Engineering at the Chinese University of Hong Kong (CUHK), under the supervision of Prof. Bei Yu since the fall of 2022. He was awarded the third prize in the CAD contest at ICCAD 2022. His research interests focus on large-scale parallelization for EDA and compilation for hardware.

Abstract: Clock gating involves inserting combinational logic along the clock path to prevent unnecessary register switching, thereby reducing dynamic power consumption.

Traditionally, clock gating is applied at Register Transistor Level (RTL) for power savings, while in a lower logical level some synthesis techniques, e.g. Observability Don't Care (ODC) can also be used to achieve further power reductions. The conditions in which the transition of a register can be safely blocked can be either explicitly specified by the designer or automatically detected. We propose an efficient logic-level clock gating scheme based on ODC conditions, aiming to reduce intramodule dynamic power in sequential circuits. This scheme is accompanied by a pruning and clustering algorithm to minimize the incurred area overhead.

16:40-17:00 | Guangyu Hu, The Hong Kong University of Science and Technology

Speech Title: Cheetah: A Parallel Word-level Model Checker

Bio: Guangyu HU received the B.E. degree in software engineering from Xiamen University, China, in 2021. He is currently pursuing the Ph.D. degree with Microelectronics, The Hong Kong University of Science and Technology, Hongkong, China. His current research interests include machine learning guided hardware formal verification and logic synthesis.

Abstract: Cheetah is property-based parallel running model checker. It contains several heuristic methods to dynamic unroll the bounds in BMC.

TECHNICAL SESSION

TS01. Latest News From Lithography

Chair: Ren Qian, Monochip

Time	13:30-15:30 | May 11, 2024	Venue	2-9 / Presidium Room

TAIK DETAILS

13:30-13:50 | Paper ID: 184 | Xiangyu Jiang, Xidian University
Speech Title: A Review of DNN and GPU in Optical Proximity Correction
Author(s): Huming Zhu, Xiangyu Jiang, Delong Shu, Xinyue Cheng, Biao Hou, Hailong You
Abstract: Optical Proximity Correction (OPC) is a resolution enhancement technique. It compensates for imaging distortions by modifying the mask patterns. In advanced nodes, inverse lithography technology (ILT) is used to produce more complex and finer mask shapes. However, ILT increases the computational complexity and runtime. In recent years, researchers have attempted to accelerate the process using GPU and improved the accuracy using deep neural networks. In the last ten years, the rapid advancement of deep neural networks has given rise to numerous OPC algorithms based on DNN. The high performance of GPU has provided a foundation for them. Finally, we summarize the key OPC technologies during this period and made projections for it in the future.

13:50-14:10 | Paper ID: 159 | Li Xie, Shenzhen Fuxin Technology Co., Ltd. & Shenzhen GWX Technology Co., Ltd.
Speech Title: Model-based OPC Extension for the Open-source Computational Lithography Library OpenILT
Author(s): Su Zheng, Gang Xiao, Ge Yan, Meng Dong, Yao Li, Hong Chen, Yuzhe Ma, Bei Yu, Martin Wong
Abstract: Optical proximity correction (OPC) is a technique to improve the accuracy of pattern transfer from the mask to the wafer in optical lithography. Model-based OPC (MB-OPC) uses mathematical models to simulate the image formation process and adjust the mask layout accordingly. In this paper,we extend the open-source computational lithography library OpenILT to support MB-OPC. The extension provides a flexible and modular framework for implementing OPC algorithms for large-scale layouts. It also supports GPU acceleration to speed up the OPC process. We demonstrate the performance and scalability of the library on different mask patterns. The experimental results show that our method can achieve more than 5 times speedup over the CPU-based MB-OPC method, while maintaining the same correction accuracy and quality. Our MB-OPC extension can provide a powerful baseline for future research on OPC.

14:10-14:30 | Paper ID: 19 | Zebang Lin, Zhejiang University
Speech Title: End-to-end Lithography Modeling Based on Process Parameters and Deep Learning
Author(s): Zebang Lin, Kun Ren, Dawei Gao, Yongyu Wu, Shibin Xu, Miaomiao Lu
Abstract: Lithography is one of the most important processes in integrated circuit manufacturing, and with the continuous advancement of technology nodes, the cost of computational lithography is also increasing. Previous studies have mostly viewed lithography system as a black box mapping from image to image, lacking guidance on process parameters and supporting experimental data when comparing experimental results. This article models the lithography system based on process parameters and deep learning, and verifies it using experimental data. The optical system combines process parameters and uses sum of coherent systems (SOCS) to reduce the computational complexity of optical simulation. The resist system takes aerial images as input and outputs binary masks. Our proposed method has a 9.36% accuracy improvement in mean intersection over union (mIOU) compared to traditional compact resist models.

14:30-14:50 | Paper ID: 27 | Hong Chen, GWX Technology
Speech Title: Inverse Lithography with Structured Sub-Resolution Assist Features
Author(s): Xiaoxuan Liu, Jiale Liu, Wenjing He, Yaojun Du, Li Xie, Yijiang Shen, Hong Chen
Abstract: With the continuous advancement of semiconductor manufacturing technology, integrated circuits now incorporate billions of mask pattern data. In the event of non-compliance with mask design rules before

manufacturing, the entire mask needs to be re-optimized to address mask rule violations, incurring significant resource and time costs. In this paper, we address mask rule violations of width, space, minimum areas during the optimization process by constructing structured sub-resolution assist features (SRAFs) and incorporating them into the optimization process of inverse lithography technology (ILT) using the level-set method. An initial mask is calculated by combining the structured SRAFS and the optical proximity correction (OPC) region of the main features which excludes the SRAFs outside of the spacing spec. Level-set based ILT is further implemented incorporating mask rule checks (MRC) and corrections during the optimization process: features with spacing violations are merged while features with width violations are expanded to a structured formation; the contour of the detected non-compliant locations are fixated, while allowing the contour of the MRC-compliant features to evolve. This ensures that features already corrected will not experience new or previously encountered violations during the subsequent optimization iterations. Upon completion of the level set optimization, structured SRAFs with fixed widths will be defined. Simulation results indicate that the inclusion of mask rule check and correction dose compromise pattern fidelity with comparable performance, it can effectively solve the problem of mask rule violation. Furthermore, by constructing structured SRAFs, mask complexity is significantly reduced.

14:50-15:10 | Paper ID: 163 | Huwen Ding, Institute of Microelectronics of the Chinese Academy of Sciences

Speech Title: A Fast Imaging Model of Plasmonic Lithography for Line/Space Patterns Based on Parameter Sweep

Author(s): Huwen Ding, Yayi Wei

Abstract: As a new and alternative lithography technology, plasmonic lithography can break through the diffraction limit of traditional lithography by exciting the surface plasmon polaritons (SPPs) to make the evanescent wave at the mask participate in imaging. The photoresist aerial image distribution of different mask patterns can be calculated by establishing an imaging model, which is the basis for understanding and further optimizing imaging. Based on the idea of machine learning and parameter sweep, a fast imaging model for plasmonic lithography is established, including periodic line/space patterns. Compared with the rigorous numerical method, the fast imaging model can greatly improve the calculation speed with high accuracy, which creates conditions for the development of computational lithography technology.

15:10-15:30 | Paper ID: 105 | Jiashuo Wang, Institute of Microelectronics of the Chinese Academy of Sciences

Speech Title: Budget Analysis of Multiple Parameters in EUV Lithography System Based on Support Vector Machine

Author(s): Jiashuo Wang, Xiaojing Su, Yayi Wei

Abstract: As one of the most critical pattern transfer technologies in semiconductor manufacturing, lithography directly affects the performance of devices or circuits. With the development of technology node, the critical dimensions of patterns are continually shrinking, which places increasingly high demands on lithography. In order to explore the influence of various parameters of scanners on the lithography results, and to provide quantitative and precise direction for the development of extreme ultraviolet (EUV) scanners, this paper proposes a methodology of budget analysis of multiple parameters based on support vector machine (SVM). First, establish a SVM classification model between parameters in lithography system and lithography results. Then, identify the parameter combinations that meet the lithography requirements according to the SVM model. Finally, calculate basic budget range for each parameter according to the statistics on the general distribution of each parameter, as well as the strict budget range according to the joint distribution between parameters. For patterns that commonly used in EUV single exposure at the 5nm technology node, we obtained the budget ranges for 8 parameters simultaneously, where the parameters come from the light source, illumination system, and projection system. Compared to the basic range of each parameter, the strict budget range of flare and dose has been reduced by more than 50%, which provides clearer goals for the development of each subsystem in EUV scanners. Since the proposed method considers the coupling effects of multiple parameters simultaneously, the results are more reliable compared to those considering the effects of every single parameter only. Furthermore, since the operations of SVM modeling and budget analysis of this method are simple and easily extendable to more parameters, this method can serve as an effective alternative for budget analysis of parameters in future research and development of EUV scanners.

TECHNICAL SESSION

TS02. The Breakthrough in Testing

Chair: Huawei Li, ICT, CAS

Time	13:30-15:50 | May 11, 2024	Venue	2-5 / Weinan Hall

TAIK DETAILS

13:30-14:00 | Invited Talk | Sybille Hellebrand, Paderborn University

Speech Title: Functional Safety and Reliability of Interconnects Throughout the Silicon Life Cycle

Author(s): Sybille Hellebrand, Somayeh Sadeghi-Kohan, Hans-Joachim Wunderlich

Invited Speaker's Bio: Sybille Hellebrand received her Diploma degree in Mathematics from the University of Regensburg, Germany, in 1986. In the same year she joined the Institute of Computer Design and Fault Tolerance at the University of Karlsruhe, Germany, where she received the Ph. D. degree in 1991. Then she was as a postdoctoral fellow at the TIMA/IMAG-Computer Architecture Group, Grenoble, France. From 1992 to 1997 she continued as an assistant professor at the University of Siegen, Germany. Before completing her Habilitation and changing to the Division of Computer Architecture at the University of Stuttgart, Germany, in 1997, she spent several months as a guest researcher with Mentor Graphics Corporation in Portland, Oregon, USA. In 1999 she moved to the University of Innsbruck in Austria as a full professor for Computer Science. During her time in Innsbruck, she was the head of the Institute of Computer Science from 2001 to 2004. Since December 2004, Sybille Hellebrand holds a chair in Computer Engineering at the University of Paderborn, Germany. From 2006 - 2011 she was also the head of the Institute of Electrical Engineering and Information Technology. In 2014 she was appointed guest professor at Hefei University of Technology in China.

Her main research interests include test and diagnosis of micro-electronic systems, in particular built-in test, built-in diagnosis and built-in repair for systems-on-a-chip and networks-on-a-chip, as well as design and synthesis of testable and reliable circuits and systems. She has published numerous papers in international conferences, workshops, and journals. Besides her activities in several program committees, she serves as an associate editor of the Journal of Electronic Testing - Theory and Applications (JETTA). From 2002 to 2009 she was a member of the editorial board of IEEE Transactions on Computer-Aided Design of Circuits and Systems.

Abstract: In many applications, for example in autonomous driving, integrated systems face stringent requirements concerning performance, power, functional safety, and reliability. This is particularly true for the on-chip communication. On the other hand, small data deviations may be acceptable within a certain range, which offers opportunities for optimization. Existing solutions for system-level interconnects comprise bus encoding for performance and power, as well as error correcting codes and periodic maintenance tests for functional safety. However, these techniques also lead to additional stress and may induce crosstalk between interconnect lines, which in turn can increase electromigration and reduce the overall lifetime of the system. In this contribution, we will show how safety and reliability considerations can be properly integrated into the design of communication and test schemes.

14:00-14:30 | Invited Talk | Hans-Joachim Wunderlich, University of Stuttgart

Speech Title: Robust Test of Small Delay Faults under PVT-Variations

Author(s): Hans-Joachim Wunderlich, Hanieh Jafarzadeh, Sybille Hellebrand

Invited Speaker's Bio: Hans-Joachim Wunderlich is Professor Emeritus of the University Stuttgart and a Life Fellow of IEEE. He received the diploma degree in mathematics from the University of Freiburg, Germany, in 1981 and the Dr. rer. nat. (Ph.D. degree) from the University of Karlsruhe in 1986. Since 1991, he has been a full professor. From 2002 to 2018, he was the director of the Institute of Computer Architecture and Computer Engineering at the University of Stuttgart, Germany. He has been associate editor of various international journals and organizer of a variety of IEEE conferences on design, test and fault tolerance of electronic systems. He has published 15 books and book chapters and around 300 reviewed scientific papers in journals and conferences. His research interests include test, reliability, fault tolerance and design automation of microelectronic systems.

Abstract: Many defects during manufacturing, operation or in the wear-out phase result in delay faults and particularly Small Delay Faults (SDF) where the additional delay of a component is smaller than the clock period. SDFs are only visible at the outputs of long paths and are especially hard to detect in circuits suffering from timing variations. Major sources of timing variations are process variations (P), voltage fluctuations (V), shifts in temperature (T), and the circuit age (A). Consequently, a robust test set must be effective for all possible combinations of operational conditions, which is rarely feasible during manufacturing. In the field, these test patterns would have to be applied as a functional test by templates or as a periodic Built-In Self-Test (BIST), which is not practical. In this contribution, techniques are discussed to minimize the number of conditions, the required test sets and the test time.

14:30-14:50 | Paper ID: 6 | Feng Shi, Semisight Information Technology Co., Ltd.

Speech Title: Revisit Reconvergence Issue in Simulation-based Observability and Testability, and its Rectification

Author(s): Feng Shi, Yutong Yao, Nan Guan, Xinjie Gao, Xiaotian Su, Nan Zhang, Zhipeng Liu

Abstract: This paper presents a highly efficient and accurate approach for detecting observability and assessing testability in contemporary logic circuits with growing size and heightened complexity, especially for MCUs or SoCs used in the automotive industry. The algorithm incorporated in this methodology also mitigates the accuracy loss caused by reconvergent fan-outs. The proposed observability correction method results in a significant improvement in rectifying erroneous node observability calculations compared to existing algorithms while achieving faster execution times. In the context of simulation-based testability and observability evaluations, we also introduce a constant folding algorithm that enables rapid MFFC calculation. By incorporating levelized data parallelism in a two-phase computation process (comprising forward and backward propagation), our approach achieves a performance speedup of more than two orders of magnitude compared to mainstream SAT solver-based techniques and is 50X faster than the fault injection engine of a commercial tool.

14:50-15:10 | Paper ID: 150 | Hongfan Zhao, GWX Technology

Speech Title: A Graph AutoEncoder Approach for Fault Prediction in Test Pattern Generation

Author(s): Hongfan Zhao, Fan Yang, Jianyuan Shan

Abstract: In System-on-Chip (SOC) testing, various fault models are created to simulate the actual behaviors of faults. Based on these models, comprehensive test patterns are generated to test the SOC thoroughly. This ensures that the SOC can identify and resolve any potential issues that may arise during its operation. ;;During the test pattern generation (TPG) process, generating a test pattern to detect part of faults can be very difficult due to various limitations, including design complexity, limited pattern search, and fault modeling. This paper refers to these types of faults as Hard-to-Detect faults (HDFs). The presence of HDFs results in a loss of test coverage and consumes significant computing resources during TPG.

15:10-15:30 | Paper ID: 180 | Yawei Jin, Xidian University

Speech Title: On Latent Defect Acceleration

Author(s): Yawei Jin, Yang Zhang, Hong Zhang, Chen Chen, Xiaoling Lin, Yongsheng Sun, Yu Huang, Cong Li, Hailong You

Abstract: With the widespread application of chips in missioncritical and safety-critical fields, ensuring that chips do not fail during operation has become crucial. However, the increasing number of hard-to-detect latent defects within chips is one of the main factors affecting the quality and reliability of the chip. In this paper, we propose a method to generate latent defect acceleration patterns based on path critical defect locations. When the latent defect appears in different defect locations of the path, the delay of the path will be affected differently. In the proposed method, defect criticality is used to measure the impact of latent defects at different locations on path delay. Critical latent defect locations of the path are selected based on the value of defect criticality. Then the user-defined-fault model (UDFM) is used to generate the latent defect acceleration pattern with the goal of maximizing the electrical activity of the critical latent defect location in the path. Experimental results show that the patterns generated using our method achieves an average of 34.9% increase in current through path critical latent defect locations compared to transition patterns.

15:30-15:50 | Paper ID: 108 | Yonghao Wang, Institute of Computing Technology, Chinese Academy of Sciences

Speech Title: Multi-dimensional Acceleration of Fault Simulation on ARM Multicore CPU

Author(s): Yonghao Wang, Zhiteng Chao, Senlin Wang, Feng Gu, Tiancheng Wang, Jing Ye, Huawei Li

Abstract: With the rapid increase in the scale of Very Large Scale Integration (VLSI), the runtime of fault simulation becomes a crucial issue during the test development phase of the VLSI design process. Various acceleration techniques have been proposed across different dimensions. However, a single technique may struggle to comprehensively address the multiple challenges in the fault simulation domain. This paper optimizes existing multi-threaded fault simulation algorithms on ARM multi-core processors. Firstly, the baseline single-threaded fault simulation algorithm was implemented with various optimization techniques such as event-driven, fault collapsing, and ARM NEON. Secondly, based on the analysis of uneven workloads in a previous multi-threaded algorithm, we present a fault-block allocation strategy to balance workloads among threads, which adopts parallel pattern single fault propagation and FFR-based fault sorting as well, to effectively reduce simulation path disparities among different threads. Experimental results conducted on the Kunpeng 920 processor demonstrate the effectiveness of the implemented algorithm with integrated multiple optimization techniques.

TECHNICAL SESSION

TS03. Advanced Tactics in Design Methodology

Chair: Peter Chun, University of Alberta

Time	13:30-15:20 | May 11, 2024	Venue	2-1 / Xianyang Hall

TAIK DETAILS

13:30-14:00 | Invited Talk | Zebo Peng, Linkoping University

Speech Title: Security-Aware Design of Cyber-Physical Systems for Control over the Cloud

Author(s): Zebo Peng

Invited Speaker's Bio: Zebo Peng received his BSc degree in Computer Engineering from the South China University of Technology in 1982, and PhD in Computer Science from Linköping University in 1987. He has been Professor and Director of the Embedded Systems Laboratory at Linköping University since 1996. He is currently also Vice-Chairman of the Department of Computer and Information Science. His research interests include the design and testing of embedded systems, electronic design automation, SoC testing, and real-time systems. He has published more than 400 technical papers and five books in these areas. He has received four best paper awards and one best presentation award at major international conferences. He has been a Golden Core Member of the IEEE Computer Society since 2005 and received the IEEE Computer Society Distinguished Contributor Award in 2022. He has served on the program committee of a dozen international conferences and was Program Chair for DATE 2008 and General Co-Chair for ITC-Asia 2021.

Abstract: Modern-day control applications increasingly rely on cyber-physical systems (CPS) to implement advanced functionalities. Notable examples within automotive domains include adaptive cruise control, intelligent navigation, and autonomous driving. Leveraging the cloud's virtually infinite storage and computational power proves to be an efficient strategy for executing these sophisticated control algorithms. However, migrating control computations to the cloud introduces new challenges, notably pertaining to security and real-time constraints. We will present an integrated design and optimization methodology tailored for cloud-based control systems. This approach addresses security concerns and other crucial CPS design prerequisites, particularly focusing on ensuring the security and stability mandates of control loops closed over the cloud.

14:00-14:20 | Paper ID: 179 | Tianyang Liu, National ASIC Center

Speech Title: ChatChisel: Enabling Agile Hardware Design with Large Language Models

Author(s): Tianyang Liu, Qi Tian, Jianmin Ye, LikTung Fu, Shengchu Su, Junyan Li, Gwok-Waa Wan, Layton Zhang, Sam-Zaak Wong, Xi Wang, Jun Yang

Abstract: With the increasing complexity of integrated circuits, agile hardware design methodologies are crucial. Modern HDLs like Chisel enhance design quality, but manual implementations remain error-prone and time-consuming. Large language models (LLMs) offer potential for design automation through natural language, but face challenges in generating large circuits using Verilog. We evaluate LLM capabilities for Chisel and Verilog generation, demonstrating superior Chisel generation ability. We introduce "ChatChisel," the first language-based agile hardware design workflow that generates Chisel from language specifications. ChatChisel utilizes four LLM-based modules for decomposing, generating, error-correcting, and composing hardware designs. Techniques like LLM collaboration and RAG enhance ChatChisel's performance. Using only GPT-3.5-turbo, we generated a RISC-V CPU supporting RV32I, pipelining, and dynamic branch prediction, validating our approach. This work automates agile hardware creation with LLMs, significantly reducing design time and improving design quality.

14:20-14:40 | Paper ID: 106 | Jienan Chen, University of Electronic Science and Technology of China

Speech Title: GraphRTL: An Agile Design Framework of RTL Code from Data Flow Graphs

Author(s): Yuheng Qiao, Cai Xie, Zhaoting Ou, Peizhi Lei, Yan Tian, Jienan Chen

Abstract: As the increasing demand for large and complex signal processing requirements, the efficient and fast design of signal processing circuits becomes an important issues. Agile design offers a new approach for rapid hardware design cycles. While this approach is a standard for software design, how to adapt it to hardware design properly remains an open question. In our work, we propose a framework for agile software and hardware co-design named GraphRTL. The tool addresses the challenge of designing hardware for Digital Signal Processing (DSP). Instead of direct coding and debugging iteration, we employ data flow graphs (DFG) and control flow graphs (CFG) to automatically generate RTL code. The input to GraphRTL is the flow graph of the designed circuit. Subsequently, the tool checks the graphs, reconstructs it, and then translates it into a configuration file for the compiler. Finally, the compiler autonomously generates the corresponding software to hardware code and RTL code. Compared to the traditional design route, GraphRTL enhances design efficiency and broadens the design space. In our experiments, we achieved up to an 70% reduction in design time while maintaining a 5 to 10% reduction in hardware overhead for the designed circuits.

14:40-15:00 | Paper ID: 92 | Lixia Han, Peking University

Speech Title: CoMN: Co-design Platform for Non-volatile Memory Based Neural Network Inference Accelerators

Author(s): Lixia Han, Siyuan Chen, Peng Huang, Xiaoyan Liu

Abstract: The interdependence of various design levels in computing-in-memory (CIM) chips makes optimization at a single level insufficient to achieve the desired performance metrics. Collaborative optimization across different design levels, including algorithms, architecture, circuits, and devices, has emerged as a requisite technique. We have developed a hardware-software co-design tool, CoMN, to facilitate rapid deployment of neural networks on CIM chips, to evaluate and trade-off accuracy and performance, as well as to explore the algorithm-hardware design space. To enhance the usability of CoMN, a graphical user interface has been developed, accessible via the URL http://101.42.97.22:8081/index.html. CoMN is designed not only to enable users to preliminarily assess their concepts without comprehensive knowledge of all CIM chip design intricacies but also to narrow down the scope of hardware optimization, thereby expediting subsequent design stages.

15:00-15:20 | Paper ID: 45 | Tao Li, Xidian University

Speech Title: Model Inference Optimization on ReRAM-Based Accelerators with Intra- and Inter-OU Similarity

Author(s): Tao Li, Qinghang Zhao

Abstract: Computing-In-Memory (CIM) technology is promising for DNN inference acceleration, in which ReRAM-based crossbars have received extensive attention in various aspects. However, the current model deployment research often neglects the read-write imbalance problem. This work proposes a comprehensive solution of inference optimization for multi-bit ReRAM-based crossbar array accelerator. In fine grain of operation unit (OU), a row and column exchange algorithm called RCSwap is proposed to minimize the difference between the weights before and after update and therefore reduce the program time and energy consumption. And in coarse grain, similarity-based scheduling method is presented to exploit the inter-OU difference for further performance improvement. Experiment results show that the proposed methods combined reduce up to 32% and 34% in time delay and energy consumption for model inference, respectively.

TECHNICAL SESSION

TS04. Transient Simulation and Model Reduction

Chair: Lining Zhang, Peking University

Time	13:30-15:30 | May 11, 2024	Venue	3-3 / Hanzhong Hall

TAIK DETAILS

13:30-13:50 | Paper ID: 10 | Hang Zhou, Southern University of Science and Technology

Speech Title: A Parallel Acceleration Technique Based on Bordered Block Diagonal Matrix Reordering for Exponential Integrator Method

Author(s): Hang Zhou, Dongen Yang, Yangfei Lin, Yong Dai, Quan Chen

Abstract: The exponential integrator (EI) method has proven to be an effective technique to accelerate transient circuit simulation. One core step of EI is the generation of rational Krylov subspace basis by the Arnoldi process, which involves one (exact) LU factorization and many back/forward triangular solves. Traditional parallelization techniques for circuit simulation perform well in accelerating the LU factorization part (the symbolic and numerical factorization) but fall short in parallelizing the triangular solution part. In this paper, we propose a parallel Bordered Block Diagonal (BBD) matrix reordering algorithm and a parallelization based on OpenMP and MPI to accelerate triangular solutions involved in the rational Krylov space construction in EI. Parallelization is achieved by solving corresponding part of solution vector of each diagonal matrix block independently. Numerical experiments shows that our method can achieve 3.3x and 1.9x speedup under shared and distributed memory environment respectively.

13:50-14:10 | Paper ID: 65 | Zijia Zhang, Southeast University

Speech Title: P-TICER: An Effective Parallel TICER Acceleration Method for Model Order Reduction

Author(s): Zijia Zhang, Dan Niu, Zhou Jin, Pengju Chen, Zhenya Zhou, Changyin Sun

Abstract: In the field of post simulation verification in integrated circuit design, Time-Constant Equilibration Reduction (TICER) is a well-known and widely used algorithm for model order reduction. However, the TICER for large-scale circuits is time-consuming. Moreover, there is a contradiction between the node compression ratio and circuit sparsity. In this paper, an effective TICER-based optimization parellel acceleration algorithm called P-TICER is proposed. An adaptive circuit judgment partitioning strategy based on graph partitioning is proposed to partition circuits and perform multi-threaded parallel acceleration. The compression ratio and sparsity of the circuit are optimized and balanced. Moreover, RC-In-RC-Out structure is designed, which is realizable and seamlessly integratable with other simulators as it takes circuit netlists as input and output. We apply P-TICER to the RC circuits with two different types and nodes scale ranging from 40k to 2 million. Experimental results show that compared with the conventional TICER, the proposed P-TICER is up to 24 times faster, while achieving a node compression ratio up to 50% with the relative error remained within 0.2%.

14:10-14:30 | Paper ID: 98 | Xiaowei Jia, Empyrean Technology Co., Ltd.

Speech Title: Implementation of Mixed Precision Sparse Matrix Solving in the Large Scale Circuit Transient Simulation

Author(s): Jingrui Chen, Minghou Cheng, Xuan Xiao, Xiaomeng Jiao, Jinyu Zhang, Xiaolue Lai, Zhenya Zhou

Abstract: We implement mixed precision sparse matrix solver in the transient simulation of analog circuits. In each time step, we need to perform one single precision LU factorization and a few steps of mixed precision iterative refinement. The overall time benefit of mixed precision sparse matrix solver is 10% compared to double precision sparse matrix solver. The sparsity of the matrix plays a significant role in improving the performance of mixed-precision computation.

14:30-14:50 | Paper ID: 103 | Xianting Lu, Zhejiang University

Speech Title: An Efficient Approach to Multiphase Constant On-Time Buck Converter Simulation

Author(s): Xianting Lu, Xunzhao Yin, Cheng Zhuo

Abstract: The growing demands on microprocessors necessitate advancements in power delivery systems, where multiphase interleaved constant on-time (COT) buck converters stand out for their fast response and high efficiency. While simulations of COT buck circuits are crucial for evaluating circuit performance comprehensively, the inherent complexities in designing these circuits present significant challenges. Particularly, COT buck circuits with an increased number of phases exhibit heightened complexity, often leading to simulation issues such as crashes, interruptions, and non-convergence. The absence of a robust and straightforward simulation structure for high-phase-number COT circuits exacerbates these challenges. To mitigate these issues, this paper introduces a novel structure for COT buck circuit modeling that is specifically designed to support phase expansion and facilitate flexible parameter adjustments for generic SPICE level simulator. This structure aims to simplify the simulation process for complex, multiphase COT buck circuits, thereby improving the feasibility and reliability of the simulations. Furthermore, to enhance the stability and performance of the multiphase COT buck circuit, we implement a current balancing technique, ensuring uniform current distribution across all phases during transient responses. Simulation results validate the effectiveness of the proposed COT buck circuit model, which demonstrates adaptability to varying circuit parameters and maintains good performance even as the number of phases increases.

14:50-15:10 | Paper ID: 131 | Xingyu Tang, Tsinghua University

Speech Title: A Wideband Behavioral Model with Multiple States for RF Power Amplifier Based on Improved Recurrent Neural Network

Author(s): Xingyu Tang, Zhikai Wang, Yan Wang

Abstract: The signal bandwidth of wireless communication systems is increasing with the advent of the fifth/sixth generation (5/6G) communication, leading to strong memory effects and nonlinearity in RF power amplifiers (PAs). Although artificial neural networks (ANNs) and deep neural networks (DNNs) perform well in PA behavioral modeling with high-dimensional inputs, the modeling accuracy and efficiency still have more room to enhance. In this paper, an improved recurrent neural network (IRNN) based PA behavioral model is presented, in which a special inter-middle layer was added between the RNN network and the MLP network to enhance the wideband modeling capability of memory effects and nonlinearity. The proposed IRNN method also introduces multiple states and the output of the RNN network and the MLP network at previous time into the input vectors, so a big improvement in behavior modeling accuracy with reasonable complexity was achieved. Compared with E-ELM, DNN, and conventional RNN methods, this method can achieve a 9.01 to 17.08 dB improvement in modeling accuracy in the form of normalized MSE (NMSE) on average without adding excessive time cost. In addition, it is shown that the model can predict the behavior of the PA under different input power levels and frequencies accurately, revealing that the new modeling methodology provides very efficient and extremely accurate prediction.

15:10-15:30 | Paper ID: 147 | Yuchao Zhong, Southeast University

Speech Title: CGAT-TICER: A Compressed GAT-based TICER for RC Reduction

Author(s): Yuchao Zhong, Yunfan Zuo, Leyun Tian, Sen Hu, Hao Yan

Abstract: Model order reduction (MOR) is an effective method to reduce the circuit simulation time. As a conventional MOR method, Time Constant Equilibration Reduction (TICER) is used widely in fast interconnect analysis. Recently GCN-TICER is proposed by converting the node elimination speed-up problem into the classification issue using GCN-based anomaly detection.However, poor accuracy of node classification leads to insufficient efficiency. Besides, numerous unnecessary computations result in the high cost of elimination due to the uncompacted model. In this paper, we propose an improved algorithm CGAT-TICER using an anomaly detection method based on Graph Attention Network(GAT) to improve the accuracy of node classification. At the same time, we discard irrelevant elements to obtain a compressed model,thus reducing the elimination time. We conduct experiments on 6cases ranging from 1,983 to 1,026,495 nodes in size from a clock_x0002_tree network. Experiments show that our algorithm achieves a1.34× to 17.23× speedup compared to TICER, which is twice the SOTA GCN-TICER. The max relative error is less than 1.106%,which is 0.124% to 0.952% larger than TICER but smaller than GCN-TICER.

TECHNICAL SESSION

TS05. Design Verification

Chair: Yun Liang, Peking University

Time	16:00-17:50 | May 11, 2024	Venue	2-6 / Baoji Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Ying J Chen, S2C

Speech Title: Design the Right Chip and Design the Chip Right with Precision Chip Strategy

Invited Speaker's Bio: Mr. Ying Jen Chen has over 26 years of product technology and market experience in the digital IC industry, with 21 years dedicated to the FPGA field. Before joining S2C, he was Asia Pacific Marketing Manager at Lattice Semiconductor. He worked at Altera Corporation for 15 years, holding various roles in technical and sales management across locations from the United States to Taiwan.

Mr. Chen graduated from the University of California, Berkeley, with dual bachelor's degrees in Electrical Engineering and Computer Science (EECS) and Materials Science and Engineering.

Abstract: Fast evovling technolies and applications such as RISC-V, Chiplet and AI are making it harder for designers to keep up with the fast changing market demands. As a leading EDA solution leader specializing in functional verfication, S2C will discuss how its Precision Chip strategy can help "Design the Right Chip and Design the Chip Right" and accelerate time-to-market.

16:30-16:50 | Paper ID: 40 | Qin He, EnnoCAD Electronics Technology Co., Ltd.

Speech Title: An Efficient Circuit Matching Algorithm Based on Hash Extraction of Features

Author(s): Qin He, Yingmeng Li

Abstract: In the field of Electronic Design Automation (EDA) tools, the identification of specific circuit configurations from a design is an inevitable requirement. This paper proposes a novel and efficient technique. Through extensive validation, the algorithm demonstrates accurate identification of specific circuit configurations. Moreover, for large designs with millions of instances, when the traversal starting point is also in the millions, the algorithm takes approximately eight hundred seconds to complete. This demonstrates a high level of efficiency.

16:50-17:10 | Paper ID: 3 | Qianwen Zhao, The Hong Kong University of Science and Technology (Guangzhou)

Speech Title: How Good is Your Property? A New Metric for Formal Property Coverage

Author(s): Qianwen Zhao, Hongce Zhang

Abstract: Formal property verification has been widely used in function verification, where user-specified properties are checked to ensure function correctness. However, as human verification engineers can also make mistakes when writing the properties, it is a general question on how to ensure the quality of formal properties. There are several existing coverage metrics, e.g., cone-of-influence (COI) and ProofCore coverage that assess the quality of properties in the setting of formal property verification. However, they are not sufficient to identify all coverage holes as this paper will show. Therefore, we propose FRCoverage, a new functional coverage metric for formal property verification, which is based on function reduction. Our case study shows that this new coverage metric successfully identifies three coverage holes in the commonly used RISCV-Formal verification framework when it is applied on PicoRV32 processor verification.

17:10-17:30 | Paper ID: 212 | Shixiong Kai, Huawei

Speech Title: Towards Smart Industrial Hardware Formal Verification

Author(s): Hui-Ling Zhen, Shixiong Kai, Min Li, Lihao Yin, Yingzhao Lian, Zhentao Tang, Haoyang Li, Junhua Huang, Mingxuan Yuan, Yu Huang

Abstract: Formal verification has emerged as an alternative approach to guaranteeing the quality and accuracy of hardware designs, surpassing the limitations of traditional validation techniques like simulation and testing. However, as the number of state variables in the system increases, the size of the system state space expands exponentially, leading to the inevitable occurrence of the state explosion problem. Unlike the academic community, which has primarily focused on verification techniques, our approach emphasizes more intelligent modeling and data-driven acceleration.

17:30-17:50 | Paper ID: 137 | Jing Tang, Xidian University

Speech Title: TBPart: An Effective Topological Order Balanced Hypergraph Partitioning Algorithm for VLSI Processor-based Hardware Emulation

Author(s): Jing Tang, Shunyang Bi, Haonan Wu, Hailong You

Abstract: As the complexity of circuit designs continues growing, processor-based emulation is becoming more and more popular for design verification. In a large-scale design, there are significant dependencies among the basic logic cells, which is represented as cells' topological order if the design is mapped to a graph. During the circuit partitioning stage, assigning the same topological order cells to one processor would significantly increase the delay of scheduling, further degrading the overall performance. However, some well-known partitioners, like hMETIS and PaToH, mainly focus on cut size minimization without considering such topological order balance constraints, which limits their practical usage in processor-based hardware emulation. In this paper, we propose a partitioning algorithm TBPart considering the topological order balance to address the issue of wasting computational resources in hardware emulation. TBPart improves the topological balance of the partitioning results by considering the gain brought by vertices movement in improving the topological balance while also taking into account the cut-size loss, ensuring the quality of the cut-size while improving the topological balance of the partitioning results. We evaluate TBPart using the ISPD98 benchmark tests, and experimental results demonstrate its effectiveness in improving the topological order balance. On average hand, 0.26 times cut-size loss can result in a 2-fold improvement in topological order balance.

TECHNICAL SESSION

TS06. The Open Source EDA Movement

Chair: Guojie Luo, Peking University

Time	16:00-18:20 | May 11, 2024	Venue	2-5 / Weinan Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Tsung-Yi Ho, The Chinese University of Hong Kong

Speech Title: Open-Source Incubation Ecosystem to Democratize Digital Microfluidics

Invited Speaker's Bio: Tsung-Yi Ho is a Professor in the Department of Computer Science and Engineering, the Chinese University of Hong Kong (CUHK). He received his Ph.D. in Electrical Engineering from National Taiwan University in 2005. His research interests include several areas of computing and emerging technologies, especially in design automation of microfluidic biochips. He has been the recipient of the Invitational Fellowship of the Japan Society for the Promotion of Science (JSPS), the Humboldt Research Fellowship by the Alexander von Humboldt Foundation, the Hans Fischer Fellowship by the Institute of Advanced Study of the Technische Universität München, and the International Visiting Research Scholarship by the Peter Wall Institute of Advanced Study of the University of British Columbia. He was a recipient of the Best Paper Awards at the VLSI Test Symposium (VTS) in 2013 and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems in 2015. He served as an ACM Distinguished Speaker for 2014-2020, a Distinguished Visitor of the IEEE Computer Society for 2013-2015, a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2016-2017, the Chair of the IEEE Computer Society Tainan Chapter for 2013-2015, the Chair of the ACM SIGDA Taiwan Chapter for 2014-2015, the Secretary General of the IEEE Taipei Section for 2019-2020, and the VP Technical Activities of the IEEE CEDA for 2020-2023. Currently, he serves as the VP Conferences of IEEE CEDA, and the Executive Committee of ASP-DAC and ICCAD. He is a Distinguished Member of ACM and a Fellow of IEEE.

Abstract: Advances in microfluidic technologies have led to the emergence of biochip devices for automating laboratory procedures in biochemistry and molecular biology. Corresponding systems are revolutionizing a diverse range of applications, e.g. point-of-care clinical diagnostics, drug discovery, and DNA sequencing–with an increasing market. However, continued growth (and larger revenues resulting from technology adoption by pharmaceutical and healthcare companies) depends on advances in chip integration and design-automation tools. Thus, there is a need to deliver the same level of design automation support to the biochip designer that the semiconductor industry now takes for granted. In particular, the design of efficient design automation algorithms for implementing biochemistry protocols to ensure that biochips are as versatile as the macro-labs that they are intended to replace. This talk will first describe technology platforms for accomplishing "biochemistry on a chip", and introduce the audience to both the droplet-based "digital" microfluidics based on electrowetting actuation and flow-based "continuous" microfluidics based on microvalve technology. Next, the presenter will describe system-level synthesis including operation scheduling and resource binding algorithms, and physical-level synthesis includes placement and routing optimizations. Moreover, control synthesis and sensor feedback-based cyberphysical adaptation will be presented. In this way, the audience will see how a "biochip compiler" can translate protocol descriptions provided by an end user (e.g., a chemist or a nurse at a doctor's clinic) to a set of optimized and executable fluidic instructions that will run on the underlying microfluidic platform. Finally, present status and future challenges of the open-source microfluidic ecosystem will be covered.

16:30-17:00 | Invited Talk | Xingquan Li, Peng Cheng Laboratory

Speech Title: AiEDA: An Open-source AI-native EDA Library

Author(s): Zhipeng Huang, Zengrong Huang, Simin Tao, Shijian Chen, Zhisheng Zeng, Liwei Ni, Chunan Zhuang, Weiguo Li, Xueyan Zhao, He Liu, Biwei Xie, Xingquan Li

Invited Speaker's Bio: Dr. Xingquan Li is an associate researcher at Peng Cheng Laboratory (PCL). He received the Ph.D degree from Fuzhou University in 2018. His research interesting includes EDA and AI for EDA. His team has developed an open-source EDA infrastructure (iEDA). He has published over 40 papers in journals and conferences such as TCAD, TC, TVLSI, TODAES, DAC, ICCAD, DATE, ICCD, ASP-DAC, and has filed 13 invention patents. He has achieved first-place award from ICCAD@CAD Contest three times in 2017, 2018, and 2022. In 2020, he was honored with the Operational Research Application Award from the Chinese Operations Research Society. In 2023, he received the Best Paper Award from ISEDA.

Abstract: Although Artificial Intelligence (AI) has made significant progress in the Electronic Design Automation (EDA) field, specialized research infrastructure remains insufficient. This paper analyzes the elements required for a better integration of AI with EDA, and presents the preliminary framework of our AiEDA library. This library aims to support AI tasks more effectively within EDA by integrating open-source tools, enhancing data management, and adding functional modules for testing and analysis.

17:00-17:20 | Paper ID: 31 | Kaichuang Shi, Fudan University

Speech Title: An Open-Source Tool to Model and Explore Complex Routing Architecture for FPGA

Author(s): Kaichuang Shi, Lingli Wang

Abstract: Routing architecture has a large impact on the FPGA performance and area. In academia, the routing architecture is mainly based on the connection blocks (CBs) and switch blocks (SBs) which is used in VPR. And there are input crossbars inside the logic blocks (LBs). The routing architecture in VPR is not tileable. Besides, it is hard to model the complex routing architecture as in commercial FPGAs. In this paper, we model a tile-based VRB (Versatile Routing Block) architecture which replaces the CBs, SBs and input crossbars to alleviate this problem. All the routing resources are included in the VRBs and many routing features which are used in commercial FPGAs are supported, such as bent wires, nearest neighbor interconnects and two-level mux topology. In addition, VTR 8 is enhanced to support the VRB architecture and we make it open publicly. Experimental results show that the proposed VRB architecture can achieve 8.2% improvement on the critical path delay and 8.4% improvement on the area-delay product compared to the latest two-level mux architecture.

17:20-17:40 | Paper ID: 129 | Hongtao Cheng, Beijing University of Posts and Telecommunications

Speech Title: SATGL: An Open-source Graph Learning Toolkit for Boolean Satisfiability

Author(s): Hongtao Cheng, Jiawei Liu, Jianwang Zhai, Mingyu Zhao, Cheng Yang, Chuan Shi

Abstract: As the first proven NP-complete problem, the Boolean Satisfiability (SAT) problem holds significant theoretical value and has wide ranging practical applications. It has also led to the development of numerous SAT-related tasks, such as MaxSAT and UNSAT Core prediction. Due to the high complexity of handling these SAT-related tasks and the natural conversion of SAT formulas into graph structures, researchers have recently developed various graph learning methods to assist in prediction. However, these methods are often experimented on different datasets, with different approaches and different tasks, making it challenging to conduct unified evaluations and develop new algorithms. In this paper, we introduce the SATGL toolkit, the first the first open-source graph learning toolkit for the SAT problem. graph learning toolkit for the SAT problem. We expect SATGL to contribute to the advancement of artificial intelligence (AI) for SAT, facilitating SAT solving and new algorithm design.

17:40-18:00 | Paper ID: 160 | Xiangchen Meng, The Hong Kong University of Science and Technology (Guangzhou)

Speech Title: FlattenRTL: An Open Source Tool for Flattening Verilog Module at RTL Level

Author(s): Xiangchen Meng, Ziyue Zheng, Yangdi Lyu

Abstract: While hierarchy in the Register-Transfer Level (RTL) makes hardware designs more readable, reusable, and scalable, a flattened design by removing the hierarchy is useful for synthesis, verification, and optimization. For example, a flattened Verilog module can help the verification tools better analyze the dependencies of signals in exact instances. Therefore, a tool to flatten the Verilog modules at the RTL level is helpful in the electronic design automation (EDA) domain. Flattening the Verilog modules is also a challenge with the ever-increasing complexity of hardware designs. According to our experiments, the existing tool to flatten Verilog modules in RTL is a proprietary tool from EDAUtils, which fails to pass the equivalence checking of the flattened module with the original modules in many benchmarks. In this paper, we proposed an innovative open-source tool called FlattenRTL to convert hierarchical RTL Verilog designs into a flattened, single-module form. FlattenRTL removes the hierarchy while preserving its functionality by employing code analysis and manipulation methods. Experimental results illustrate that the flattened modules pass equivalence checking in all benchmarks. In addition, FlattenRTL is more efficient than the existing proprietary Verilog flattening tool.

18:00-18:20 | Paper ID: 57 | Jing Mai, Peking University

Speech Title: OpenPARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions

Author(s): Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang, Yibo Lin

Abstract: FPGA macro placement exerts a significant influence on routability and timing closure in FPGA physical design. Macros could subject to cascaded macro constraints and necessitate placement in contiguous sites. Meanwhile, instances could also subject to fence region constraints, permitting placement within designated areas. Such kind of heterogeneity exacerbates the solution space discontinuity and leads to divergence and local optima entrapment. In this work, we propose a robust multi-electrostatics-based FPGA macro placer OpenPARF 3.0 that can handle the aforementioned constraints efficiently. We adopt a novel multi-electrostatics region model to handle the fence region discontinuity and propose a divergenceaware density weight scheduling scheme that can address the robustness issues effectively. Experimental results demonstrate that our proposed framework can address robustness issues effectively and outperform state-of-the-art placers in both quality and efficiency.

TECHNICAL SESSION

TS07. Leveraging Machine Learning in EDA

Chair: Bei Yu, The Chinese University of Hong Kong

Time	16:00-18:20 | May 11, 2024	Venue	2-1 / Xianyang Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Peter Chun, University of Alberta

Speech Title: The Synergy Between AI/ML and EDA

Invited Speaker's Bio: Peter Chun currently serves as an Adjunct Professor in the ECE department at the University of Alberta, where he is involved in AI4EDA projects and interested in AI/ML deployments in devices and holds a position of Director, technical planning and collaboration in Huawei Canada where he has initiated and managed more than 60 collaboration projects with multiple universities, and have played key roles in the technical committees (MLperf/MLC, RISC-V, GSMA TSGAI and IRDS SA) and the advisory boards (CMC and COHESA). Peter had worked with various companies Nortel, MDA, RAMBUS, Huawei where he worked on the first 40G SONET/Ethernet Metro optical systems, next generation Canadarm, RADARSAT constellation mission system, real-time video transport stream systems, mobile Image Sensor Processing units, 5G and Kunpung processor respectively.

Abstract: The Machine Learning (ML) is shown to be phenomenal for "prompting" (ChatGPT). But, it has also shown its promise to design computer systems. This interdisciplinary trend requires collaboration and furthermore foster unified methodologies between the ML and industry applications. My talk lists various examples of these attempts and how new features of ML might shine the lights on what we should focus on steming from my experience of running many collaboration projects. The talk will also premiere Dr. Matthew Taylor's vision (a short video clip) how the AI/ML (RL) can enhance the EDA solutions.

16:30-17:00 | Invited Talk | Hui-Ling Zhen, Huawei, Hong Kong

Speech Title: LLM for Better Solver and Solver for Better LLM

Invited Speaker's Bio: Dr. Hui-Ling Zhen is a principle research staff in Noah's Ark Lab, Huawei, Hong Kong. Before that, she is a post-doctoral research fellow in City University of Hong Kong, after she received the Ph.D degree in applied mathematics. Since joining Huawei, she has participated in the developments of mathematical programming solver, automatic test vector generation, logical equivalence testing, and model checking. She is also working on the research of next-generation EDA-tool enabled by LLM. Unitl now, she has published over 60 peer-reviewed papers in mainstream conferences and journals.

Abstract: Recently, Large Language Models (LLMs) have demonstrated their capability in context understanding, logic reasoning, and answer generation. In this talk, we hope to discuss whether and how to combine LLM and solver as a better combination for better reasoning and good performance. On one hand, to make use of LLMs' capability of code understanding and implementation in software, we propose BetterV, which fine-tunes LLMs on processed domain-specific Verilog datasets and incorporates generative discriminators aiming at guiding the particular design demands. As far as we know, this is the first work which gives a downstream-task-friendly verilog generation, and extensive experiments have demonstrated that BetterV outperforms GPT-4 on the VerilogEval-machine benchmark, and comparing other LLMs, it can lead to the netlist node reduction for synthesis and verification runtime reduction with SAT solving. Meanwhile, we also propose LLM as a helper in debugging. On the other hand, to improve LLM's logic reasoning ability, we propose to introduce a solver as a new layer of the LLM to differentially guide solutions towards satisfiability. Leveraging MaxSAT as a bridge, we define forward and backward transfer gradients, enabling the final model to converge to a satisfied solution or prove unsatisfiability. Experiments show that SoLA can outperform against existing symbolic solvers (including Z3 and Kissat) and tool-learning methods.

17:00-17:20 | Paper ID: 182 | Xiangru Chen, IMT Mines Ales

Speech Title: A Survey of Reinforcement Learning for Electronic Design Automation

Author(s): Huming Zhu, Xiangru Chen

Abstract: With the technological evolution of fabrication processes, the complexity of integrated circuit design has increased accordingly. Engineers are considering integrating machine learning techniques into the Electronic Design Automation (EDA) domain to assist in enhancing product performance and minimizing power consumption in the face of Moore's Law limitations. Reinforcement Learning (RL), as a branch of machine learning, has garnered attention in recent years. This paper provides a brief overview of RL in conjunction with EDA technology, outlining in detail the application scenarios of RL within EDA.

17:20-17:40 | Paper ID: 188 | Yangbo Wei, Southeast University

Speech Title: Knowledge Transfer for GaN HEMTs Parameter Extraction Based on Hybrid Model

Author(s): Yangbo Wei, Wei Xing, Ting-Jung Lin, Lei He

Abstract: Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) offer advantages such as wide bandgap and high electron mobility. Design of a circuit with GaN requires a highly accurate equivalent circuit model, which requires a computationally expensive parameter extraction process. Despite the success of the optimization-based parameter extraction, they are generally designed to work for individual cases, leading to inferior performance. To resolve this challenge, we harness modern AI techniques to significantly boost this cumbersome process. More specifically, we enhance the conventional optimizationbased method with three novel modifications: steps: (1) datadriven calibration for classic initialization methods with empirical equations; (2) adaptive search space for refining search space with faster searching speed and more accurate solution; (3) extracted parameters embedding using deep kernel learning for higher accuracy. The experimental results show that our proposed method reduces the optimization time by 5× and has a 1.18× accuracy improvement compared to competing methods.

17:40-18:00 | Paper ID: 20 | Yifan Zhang, Southeast University

Speech Title: Uncertainty Quantitative Analysis of MEMS Sensors Based on Physical Guided Deep Learning

Author(s): Yifan Zhang, Wenxin Zhang, Zikun Ni, Linfeng Zhao, Zaifa Zhou

Abstract: A Physical Guided Deep Learning method has been developed for MEMS uncertainty analysis. By construct a novel loss function for the neural network training, the physical constraints are added to the deep learning model. Thus, the accurate surrogate model of MEMS sensors can be established with fewer samples and the hidden features of complex models are captured by multi-hidden layers. Using a kind of vacuum sensor as the validation case, the proposed algorithm produces highly accurate analysis results and requires only 50% to 70% of the training data needed for traditional deep learning. This technique provides an effective tool for yield analysis and optimal design of MEMS devices.

18:00-18:20 | Paper ID: 96 | Yi Feng, Southeast University

Speech Title: GOMARL: Global Optimization of Multiplier Using Multi-Agent Reinforcement Learning

Author(s): Yi Feng, Chao Wang

Abstract: In modern computing, multipliers play a crucial role in enhancing the performance and efficiency of various computational tasks. Due to the extensive design space and high circuit complexity of multipliers, it is challenging to optimize the circuit structure. Previous research tends to optimize only part of the circuit in multiplication, ignoring further global optimization. Recently, reinforcement learning (RL) has shown promise in various fields of electronic design automation(EDA), including digital circuit design. In this paper, inspired by multi-agent reinforcement learning theory, a multi-agent RL(MARL) based framework is proposed, our main work involves the following aspects:(i) for compression tree in multiplier, we design a fine-grained matrix-based representation and a corresponding Q-learning based RL environment; (ii) by combining existing RL model on adder and our model on compression tree, we propose a multi-agent reinforcement learning (MA-RL) based framework, in which two agents cooperate with each other to achieve the overall optimization of multiplier in terms of area and delay. Experimental results show that the multipliers optimized by GOMARL can improve delay by more than 7% and area by more than 5% compared with baseline designs.

TECHNICAL SESSION

TS08. Multi-Physics Analysis and Simulation

Chair: Hongliang Lv, Xidian University

Time	16:00-18:20 | May 11, 2024	Venue	3-3 / Hanzhong Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Xiaohua Ma, Xidian University

Speech Title: Recent Progress and Prospects of GaN-on-Si RF Technology: High Performance Device, CMOS-compatible Fabrication Process, and III-V/CMOS Integration

Invited Speaker's Bio: Prof. Xiaohua Ma received the B.S. degree in Physics of Semiconductor Devices from Xidian University, Xi'an, China, in 1996, and the Ph.D. degree in Microelectronics and Solid-State Electronics from Xidian University in 2007. He is currently a professor and the Executive Director with the Faculty of Integrated Circuit, Xidian University. Prof. Ma has been conducting R&D work on nitride-III semiconductor technologies. His research is currently focused on developing GaN device technologies for high-frequency and high-power applications. Prof. Ma has been granted more than 40 patents on GaN electron device technologies, and published more than 500 papers in international journals, including ACS Nano, Nano Energy, Small, IEEE Electron Device Letters, Applied Physics Letters, IEEE Transactions on Electron Devices.

Abstract: GaN-based RF power technology possess the advantages of high frequency, high output power, and high efficiency, making it essential for national defense and wireless communication base station applications. While the next-generation wireless communication will operate at higher frequency with wider bandwidth and multi-mode communication than what they are now, this work puts forward that broadband and high-efficiency GaN-based RF technology can be used for terminal equipment as well as base station applications. This innovation will remarkably reduce the desired RF chips and their power consumption compared with the commonly used stack-chips method. In this work, we achieve high-efficiency GaN-based enhancement-mode RF devices suitable for terminal equipment by solving some critical issues involving design, CMOS-compatible process, and theory. We believe this work will make great contribution to the development of GaN RF technology for the next-generation wireless communication terminals or individual combat equipment in the future.

16:30-17:00 | Invited Talk | Huanhuan Zhang, Xidian University

Speech Title: Electromagnetics-Centric Multi-Physics Simulation Algorithms and Applications

Author(s): Huanhuan Zhang

Invited Speaker's Bio: Huan Huan Zhang (Senior Member, IEEE) received the Ph.D. degree in electromagnetic fields and microwave technology from the Nanjing University of Science and Technology, Nanjing, China, in 2015. He was a Post-Doctoral Research Fellow with the Center of Electromagnetics and Optics, The University of Hong Kong, Hong Kong, from 2015 to 2016. He is currently an Associate Professor with the School of Electronic Engineering, Xidian University, Xi'an, China. His current research interests include Multiphysics Simulation, Computational Electromagnetics, EMC/SI/PI, Antenna Design.

Dr. Zhang serves as the reviewer of the IEEE Transactions on Antenna and Propagation, Communications in Computational Physics, IEEE Antennas and Wireless Propagation Letters, IEEE Microwave and Wireless Components Letters, IET Radar, Sonar, Navigation, Applied Computational Electromagnetic Society Journal, etc. He was the recipient of the 2019 Young Scientist Award of the International Applied Computational Electromagnetics Society Symposium. He is also the recipient of the 2024 Young Scientist Award of Photonics and Electromagnetics Research Symposium.

Abstract: Multi-physics field coupling refers to the physical phenomenon where two or more physical fields

(such as electromagnetic, thermal, mechanical, acoustic, etc.) interact and mutually influence each other within a system. This phenomenon is commonly found in nature and practical engineering applications. For instance, the increase in integration density and power density of high-speed radio frequency integrated circuits can lead to issues such as circuit temperature rise and structural deformation, posing challenges to thermal management and structural reliability. Similarly, high-power microwave devices may experience heating due to material losses during operation, causing changes in material electrical parameters and structural deformation, significantly impacting the reliability and stability of the device's electrical performance. In the case of high-power phased-array radar antennas, improper thermal design can result in thermal deformation of the antenna array, deviation in the positions of radiating units, and deviations in electromagnetic metrics such as radiation patterns and gain from the design requirements.;;Addressing these issues urgently requires the cross-fusion of electromagnetic computation technology with other physical field computation technologies, conducting research on electromagnetics, circuits, thermal, and mechanics multi-physics field simulation techniques. This report first introduces multi-physics simulation algorithms centered around electromagnetics, detailing the equations for each physical field, boundary conditions, numerical solving methods, multi-physics field coupling mechanisms, parallel acceleration techniques, etc. It explains how to efficiently and accurately analyze multi-physics field coupling problems using limited computational resources. Subsequently, the report introduces the application of the multi-physics simulation programs developed in-house in complex engineering fields such as integrated circuits, microwave devices, antennas, and more.

17:00-17:30 | Invited Talk | Xiaoyan Liu, Peking University

Speech Title: Multi-physics Simulation of the Electromigration for Reliability Prediction

Invited Speaker's Bio: LIU, Xiaoyan received the B.Sc., M.Sc. and PhD. from Peking University in 1988, 1991 and 2001 respectively. She is currently a professor in the School of Integrated Circuits, Peking University and served as the Vice Dean. Her research interests include modeling and simulation of physical phenomena in the field of microelectronics. She has published more than 200 research papers coauthored 1 book on microelectronics.

Abstract: The electromigration (EM) reliability of interconnects becomes more and more challenging in high-density integration. EM is a typical multi-physics effect of the current driven degradation that forms void due to the mass transport in interconnects. It's strong temperature dependence and sensitive to the process integration including line dimension, interface, grain size, and the complex stress distribution of multilayer interconnect. Usually the time-to-failure (TTF) of EM is projected by the empirical prediction equations. However, the conventional empirical equation would overestimate the time-to-failure (TTF) of EM due to not taking some microscopic physical effects into consideration especially in advanced technology nodes. Hence the method to predict EM degradation accuracy and efficient is important to the robust IC design.

We developed a 3D KMC simulator to simulate the EM behaviors in multi-layer interconnects based on the microscopic mechanisms during EM including the metal ions activation, hopping and aggregation processes. The effects of e-wind, hydrostatic stress and SHE on EM are implemented in the simulator. The microscopic mechanism of EM includes the physical processes of metal ions activation, hopping and aggregation. The hopping directions are dominated by the e-wind which can be hindered by the stress- and electric field-induced back flow. The electrical properties of interconnects are calculated by the developed 3D-resistor network. The initial parameter input depends on the simulated metal material, structure and size. Once the ions distribution is changed, the potential and current would be updated. The simulator visualizes the void microscopic evolution and investigates the resistance-time degradation during EM as well as the prediction of TTF. The simulation results are agreed with the measured resistance-time curves and cumulative failure distribution respectively. Based on the simulation method, we further developed a physics-based compact model to predict the EM failure of interconnects. The proposed model includes the physical mechanisms of microscopic movements including the metal ions migration and vacancies generation, and describes resistance evolution of metal lines corresponding to the microscopic movements. The modeling resistance evolution of metal lines reveals the resistance changes undergo the three stages: the vacancies accumulation, void formation and full void growth, which agree well with the experimental data and our EM simulation. The impacts of different interconnect structures on EM degradation including aspect ratio and grain size can be analyzed. The recovery effect and

time-to-failure (TTF) of EM can be calculated by considering different interconnect structures, operation schemes and temperature. And the EM lifetime of interconnects can be predicted under DC and pulse operation by considering the recovery effect. The model can be used to analyze the EM lifetime under both DC and pulse operation conditions, and find the failure location in multilayer interconnects.

The simulation method and the compact model we developed, provide the powerful tool for assessment of the interconnect structure and prediction EM reliability in large-scale integrated circuits, especially for the advanced technology nodes.

17:30-18:00 | Invited Talk | Wenchao Chen, Zhejiang University

Speech Title: Quantum Transport and Drift-Diffusion Transport Simulation of Advanced Electronic/Optoelectronic Devices

Author(s): Wenchao Chen

Invited Speaker's Bio: Dr. Chen is a research professor with ZJU-UIUC Institute, Zhejiang University. He received the Excellent Youth Grant of Natural Science Foundation of China (NSFC) in 2021, the Outstanding Youth Grant of Natural Science Foundation of Zhejiang province in 2019. Dr. Chen received the Ph.D. degree in electrical and computer engineering from the University of Florida, Gainesville, FL, USA, in 2014. His research interests include multi-physics computation methods and their applications for micro/nano-scale electronic devices and advanced integrated circuits.

Abstract: A variety of advanced device fabrication technologies have been developed to meet the requirements of improving the performance and increasing the integration density of integrated circuit. The device size is being reducing through increasing the gate control by introducing the well-known structure like FinFET, gate-all-around (GAA) transistor, which are widely used due to their strong gate controllability, excellent performance. Since the advanced field effect transistors are in nanoscale, the carrier transport inside should be treated quantum mechanically.In this Invited Talk, simulation methods for quantum transport in FinFET, GAA FET will be presented and discussed. Moreover, time-dependent quantum transport simulation for GAA FET to explore its performance limit will be discussed. We use the explicit staggered finite difference time domain method (FDTD) to solve time-dependent Schrödinger equation. The upper limit of3dB bandwidth and intrinsic cutoff frequency, which are very important parameters of the amplifier applications, can be obtained.

On the other hand, as the integration density keeps increasing, the elevated lattice temperature due to self-heating intensifies the thermal stress effects on the transistor. The thermal stress can affect the band structure of the semiconductor material, and further induce the variations of device characteristics. In this talk, a comprehensive Multiphysics modeling and simulation of the self_x005f_x005f_x005fheating induced thermal stress effects on quantum transport in advanced FinFET will be presented.

Furthermore, drift-diffusion transport simulation methods for micrometer scale electronic and optoelectronic devices will be discussed, such as GaN transistor, photodetector and modulator. For some special devices in which both the drift-diffusion transport and quantum transport exist, the simulation becomes more complex, which will also be presented and discussed in this Invited Talk.

18:00-18:20 | Paper ID: 196 | Ruixin Liu, Xidian University

Speech Title: Design and Optimization of Water Droplet Interconnect Structures for Millimeter-Wave Band Applications

Author(s): Ruixin Liu, Junqin Zhang, Cong Wei, Guangbao Shan

Abstract: The arrival of the 5G era has led to the widespread use of millimeter waves. However, discontinuities in the vertical interconnect structure within the millimeter wave band can lead to significant impedance mismatch issues, resulting in serious loss problems. In this paper, a droplet-shaped vertical interconnect transition structure based on HTCC substrate is designed to reduce loss. Optimizing the parameters of pads and anti-pads, as well as the structure itself, by analyzing parasitic capacitances. Finally, the implementation of a rectangular anti-pad structure achieves impedance matching. Simulation results show that the return loss is less than 22 dB and insertion loss is less than 0.18 dB in the range of 28-33 GHz, which provides excellent transmission performance and can be used for the design of millimeter-band components.

TECHNICAL SESSION

TS09. New Frontiers in Analog EDA

Chair: Fan Yang, Fudan University

Time	16:00-18:10 | May 11, 2024	Venue	2-9 / Presidium Room

TAIK DETAILS

16:00-16:30 | Invited Talk | Xuan Zeng, Fudan University (Online)

Speech Title: High-Dimensional Analog Circuit Synthesis Based on Gaussian Process Enhanced Subspace Derivative Free Optimization

Invited Speaker's Bio: Xuan Zeng (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Fudan University, Shanghai, China, in 1991 and 1997, respectively. She was a Visiting Professor with the Department of Electrical Engineering, Texas A&M University, College Station, TX, USA, in 2002, and the Microelectronics Department, Technische Universiteit Delft, Delft, The Netherlands, in 2003. From 2008 to 2012, she was the Director of the State Key Laboratory of Application Specific Integrated Circuits (ASIC) and Systems, Fudan University, where she is currently a Full Professor with the Microelectronics Department. Her current research interests include analog circuit modeling and synthesis, design for manufacturability, high-speed interconnect analysis and optimization, and circuit simulation. Prof. Zeng received the Changjiang Distinguished Professor with the Ministry of Education Department of China in 2014, the Chinese National Science Funds for Distinguished Young Scientists in 2011, the First-Class of Natural Science Prize of Shanghai in 2012, the 10th For Women in Science Award in China in 2013, and the Shanghai Municipal Natural Science Peony Award in 2014. She also received the Best Paper Award from the 8th IEEE Annual Ubiquitous Computing, Electronics and Mobile Communication Conference 2017. She is an Associate Editor of the IEEE Transactions on Circuits and Systems—Part II: Express Briefs, the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, and the ACM Transactions on Design Automation of Electronic Systems.

Abstract: The existing optimization methods for analog circuit optimization, such as Bayesian Optimization and Trust Region based Derivative Free Optimization, suffer from underfitting surrogate models in high-dimensional problems, which leads to inefficient optimization and sub-optimal solutions. We present a novel Gaussian Process enhanced Subspace Derivative Free Optimization method to solve high-dimensional analog circuit optimization problems. High-dimensional promising region is reduced to a 2-D subspace with two pattern vector: the approximate gradient pattern vector and the iterative descent pattern vector. The Gaussian process is used to approximate the gradient pattern for subspace establishment, significantly enhancing the simulation efficiency. A trust region based derivative free optimization method is proposed for exploiting promising regions in effective low-dimensional subspace. The effectiveness of the proposed method is demonstrated on real-life analog circuits, achieving significant simulation number speedup and runtime speedup compared with the state-of-the-art optimization methods.

16:30-16:50 | Paper ID: 172 | Wenzhao Sun, Fudan University

Speech Title: KIDEA: A Novel Multi-Objective Optimization Algorithm and its Application in Analog Circuit Design

Author(s): Wenzhao Sun, Wangge Zuo, Bijian Lan, Qing Peng, Liqian Zhang, Jing Wan

Abstract: Conventional NSGA-II encounters significant difficulties in automatic tuning of design parameters for analog circuit design. In response, We present KIDEA, an enhancement of NSGA-II through differential evolution, Isolation Forest, and KMeans clustering. Differential evolution improves efficiency and convergence, while Isolation Forest and KMeans jointly elevate the quality of pareto optimal solutions by refining outlier detection

and solution clustering. The algorithm is used to tune the design parameters in analog circuit design. Compared to conventional NSGA-II, the results from KIDEA show average dominance improvement of 34.0% and convergence rate improvement of 3.14 times.

16:50-17:10 | Paper ID: 185 | Wangge Zuo, Fudan University

Speech Title: RLCkt Ⅱ: Deep Reinforcement Learning via Attention-Aware Sampling for Analog Integrated Circuit Transistor Sizing Automation

Author(s): Wangge Zuo, WenZhao Sun, Bijian Lan, Jing Wan

Abstract: The sizing of circuit transistors that meet design specifications in analog integrated circuit (IC) traditionally relies on the intuition and experience of human experts, posing challenges that are labor-intensive and time-consuming, particularly as circuit complexity increases. Compared to mainstream optimization algorithms that exhibit slow optimization speeds and unstable solutions when dealing with large-scale analog IC, this study introduces RLCktII, a breakthrough improvement built upon the advanced RLCkt. For the first time, it incorporates an attention mechanism combined with deep reinforcement learning into the domain of automated analog integrated circuit transistor sizing. Through the attention mechanism, it dynamically discerns the most distinctive input data, enhancing the deep reinforcement learning model's capability to handle complex tasks. RLCkt II was evaluated on two industrial scale analog integrated circuits: LDO and R2R. After one and a half days of training, our RLCkt II agent achieved an average improvement of 28.71% and 7.94% in convergence accuracy over the state-of-the-art RLCkt. In the same design tasks, RLCkt II demonstrated a speed advantage nearly a hundred times faster than the Genetic Algorithm (GA) while also ensuring greater design precision.

17:10-17:30 | Paper ID: 51 | Jiaquan Jiang, Xiamen University

Speech Title: Automated Design of a Strong-ARM Dynamic Comparator

Author(s): Jiaquan Jiang, Qingsen Wu, Yuan Wang, Qian Qin, Jinglei Hao, Chenkai Chai, Yukai Lu, Jiwen Huang, Lin Li, Zuochang Ye

Abstract: This paper presents an automated design method for a Strong-ARM dynamic comparator. By modeling and analyzing, the dynamic characteristics of the dynamic comparator are fitted into static characteristics, which is suitable for automatic sizing design with gm/ID method. The sizes of the transistors could be calculated by modeling the relationship with the specifications of the comparator, e.g., clock rate, power and input offset voltage. Furthermore, the automation process is implemented through an analog design tool Tsinghua Electronic Design (TED) and the design flow of the Strong-ARM dynamic comparator was verified at 40nm, 65nm and 180nm technologies respectively. Compared to the performance specifications and simulation results of the input offset voltage and power consumption, the maximum errors are approximately 3% and 6%. Among them, the three sets of power consumption obtained from simulation are all lower than the performance specifications.

17:30-17:50 | Paper ID: 152 | Jinyi Shen, Fudan University

Speech Title: Topology Optimization of Operational Amplifiers Using A Performance-aware Representation

Author(s): Jinyi Shen, Fan Yang, Li Shang, Changhao Yan, Zhaori Bi, Dian Zhou, Xuan Zeng

Abstract: The automatic synthesis of operational amplifiers (opamps) is in high demand to meet the diverse performance requirements of a wide range of analog circuit applications. However, existing opamp topology synthesis methods neglect circuit performance while generating circuit representations, resulting in suboptimal efficiency. To address this issue, this paper proposes a novel opamp topology optimization approach based on a performance-aware topology representation. Specifically, topology information is captured using a customized graph neural network (GNN), while performance information is incorporated by training the GNN for performance prediction through supervised learning. By combining this performance-aware representation with the genetic algorithm, an efficient opamp topology optimization method is developed. Experimental results demonstrate that our approach outperforms state-of-the-art methods in terms of both optimization efficiency and results.

17:50-18:10 | Paper ID: 168 | Peng Dong, Fudan University

Speech Title: Automated Design of Analog Circuits Based on Parallel Trust Region Bayesian Optimization

Author(s): Peng Dong, Ruiyu Lyu, Chunxi Wang, Jiale Chen, Linfeng Jiang, Cunqing Lan, Zhaori Bi, Changhao Yan

Abstract: Traditional optimization algorithms suffer performance decline in high-dimensional optimization problems, such as analog circuit design optimization. Adapting existing algorithms to parallel computing environments is a critical challenge. Therefore we propose a parallel Trust Region Bayesian Optimization(TuRBO) algorithm. This algorithm operates in parallel on different trust regions, utilizing a Multi-Armed Bandit algorithm for intelligent sampling to accelerate parameter optimization. Circuit experimental results demonstrate the advantages of this algorithm. Compared to Differential Evolution, Particle Swarm Optimization, Naive Bayesian, High-Dimensional Batch Bayesian Processing, and TuRBO algorithms, the circuit performance achieves improvements ranging from 3.7% to 98.2%. Compared to TuRBO, it achieves acceleration ratios in terms of iteration numbers ranging from 1.19× to 1.31×, and in terms of algorithm runtime ranging from 1.21× to 2.25×.

TECHNICAL SESSION

TS10. Advanced in EMIR and Parasitic Extraction

Chair: Qing He, Phlexing

Time	13:30-15:20 | May 12, 2024	Venue	3-3 / Hanzhong Hall

TAIK DETAILS

13:30-14:00 | Invited Talk | Wenjian Yu, Tsinghua University

Speech Title: Deep Learning Inspired Capacitance Extraction for IC Interconnects

Invited Speaker's Bio: Dr. Wenjian Yu is a Full Professor with the Department of Computer Science and Technology, Tsinghua University, Beijing, China. His current research interests include physical-level modeling and simulation techniques for IC design, high-performance numerical algorithms, and big-data analytics. Dr. Yu has coauthored four books and over 200 papers in refereed journals and conferences. He was the recipient of the distinguished Ph.D. Award from Tsinghua University in 2004, the Excellent Young Scholar from NSFC in 2014, and the 2nd-Class Science and Technology Award from CCF in 2022. He received the Best Paper Awards of DATE'2016, ACES'2017 and ICTAI'2019, and 8 Best Paper Award Nominations on prominent EDA conferences including ICCAD, DATE, ASPDAC, GLSVLSI and ISQED.

Abstract: In this talk, I'll review the research progress on IC capacitance extraction, especially the usage of deep-learning technologies in the relevant problems. Firstly, a method based on GNN for predicting the capacitance parasitics in the pre-layout design stage is presented. It exhibits potential benefit for the design optimization of some specific circuits like SRAM. Then, the deep-learning-inspired methods for post-layout capacitance extraction are presented. They can revamp the accuracy drawback of layout parasitic extraction (LPE) method and efficiency drawback of 3-D capacitance field solver. These methods include CNN-Cap, GNN-Cap and NAS-Cap. Lastly, I'll briefly review the progress on the random walk based 3-D capacitance solver, especially the deep-learning-aided technique for improving its accuracy for the structures under the advanced process technology.

14:00-14:20 | Paper ID: 115 | Yuyao Liang, Shenzhen University

Speech Title: PCT-Cap: Point Cloud Transformer for Accurate 3D Capacitance Extraction

Author(s): Ye Cai, Yuyao Liang, Zhipeng Luo, Biwei Xie, Xingquan Li

Abstract: Accurate parasitic capacitance extraction becomes increasingly essential in advanced technology nodes. 2.5D extraction requires more effort to maintain accuracy comparable to the 3D solver. In this work, two experiments reveal that error deviation in the 2.5D method enlarges as wire width shrinks and length increases. A novel Gauss law-based point cloud is proposed to model the 3D capacitance problem. With the proposed data representation, a transformer-based neural network architecture, called PCT-Cap, is designed for 3D pattern matching. PCT-Cap exhibits much better performance than the ResNet-based capacitance models. Extensive experiments on 28nm technology demonstrate that PCT-Cap can accurately predict over 95.41% of total capacitance with an error margin of less than 5%. Additionally, PCT-Cap achieves 95.90% accuracy in predicting coupling capacitance within a margin of error of less than 10%. PCT-Cap achieves at least a 55 times speeding up compared with the commercial extraction tool while consuming negligible memory.

14:20-14:40 | Paper ID: 97 | Wenjie Zhu, Shanghai Jiao Tong University

Speech Title: Fast Electromigration Stress Evolution Analysis Based on Relative Gain Array

Author(s): Zixuan Meng, Xiaoman Yang, Yuhan Zhang, Wenjie Zhu, Tianshu Hou, Hai-Bao Chen

Abstract: As technology moves to smaller feature sizes and interconnect current densities continue to increase, electromigration (EM) poses a significant challenge to the reliability of the large integrated circuit design. In order to improve the efficiency of the EM stress analysis for any general interconnect or power grid, we introduce

an efficient electromigration analysis approach based on decentralized model order reduction (MOR). Initially, the original Multi-Input Multi-Output (MIMO) system obtained by discretization is decoupled into a series of Multi-Input Single-Output (MISO) subsystems through the application of the Relative Gain Array (RGA) matrix. Subsequently, each subsystem is reduced by MOR techniques, thereby obtaining the reduced low-order subsystem corresponding to the certain output port for EM stress evolution analysis. By conducting simulations and numerical calculations on the resulting subsystem, the calculation efficiency can be greatly accelerated while maintaining the accuracy of EM transient analysis. Experiments demonstrate about 11X-187X speedup over COMSOL and about 11X-32X speedup over the standard transient analysis of original system, while the error is almost negligible.

14:40-15:00 | Paper ID: 109 | Jitao Yu, Southeast University

Speech Title: UCMNet: Static IR Drop Estimation Using Attention Convolutional Network

Author(s): Jitao Yu, Huan Liang, Shuhao Jia, Chuanfang Jiang, Aiguo Bu

Abstract: In the current chip design flow at advanced process nodes,IR drop analysis is a critical step in chip signoff, which requires expensive computation and a long time. In this work, we propose a machine learning (ML) model based on improved convolutional neural networks (CNN). It takes multiple maps of the full-chip design and features of instances as input, enabling rapid and accurate estimation of instance-level static IR drop. Experimental results show that the model achieves 330X speedup compared to existing commercial tools, with high average CC values (0.9737) and low average MAE values (0.6833mv). Furthermore, compared to existing ML methods the maximum improvement in accuracy can reach 87.2%.

15:00-15:20 | Paper ID: 194 | Zhengfei Qi, China University of Petroleum

Speech Title: UnetPro: Combining Attention with Skip Connection in Unet for Efficient IR Drop Prediction

Author(s): Zhengfei Qi, Wanchao Wang, Chengxuan Yu, Dan Niu, Xiao Wu, Zhou Jin

Abstract: IR drop analysis plays a key role in chip design. Unlike conventional time-consuming numerical analysis methods, which involve solving large-scale linear circuit equations, predicting the IR drop with machine learning shows great potential to significantly reduce computation time. However, applying machine learning for accurate prediction is non-trivial since achieving effective feature extraction poses significant challenges. Furthermore, as the number of layers in the neural network model increases, the loss of information in the transmission process gradually increases, leading to inaccurate prediction results. In this paper, we propose UnetPro, an innovative machine learning model to resolve these challenges. We leverage an attention mechanism that combines both global and local information and a multi-scale convolution module to make the model sufficiently perceive the various regions of the feature map, enhancing the feature extraction ability of the model. Moreover, we ensure the coherence of information by introducing skip connection. We also introduce the dropout mechanism to ensure the stability of model with information transfer. Compared with conventional Unet model, the error and correlation of our proposed algorithm are lower than it by 2.5e-4 and higher by 10.34%, respectively.

TECHNICAL SESSION

TS11. Co-Optimizing Systems, Design, and Technology

Chair: Xingsheng Wang, Huazhong University of Science and Technology

Time	13:30-15:30 | May 12, 2024	Venue	3-6 / Yulin Hall

TAIK DETAILS

13:30-14:00 | Invited Talk | Gordon Shou, Zhejiang ICsprout Semiconductor Co., Ltd.

Speech Title: New AI Approach of Foundry-based DTCO Methodology for Next-Generation EDA Applications

Invited Speaker's Bio: A seasoned semiconductor industry veteran, Gordon Shou holds nearly 3decades of comprehensive experience spanning engineering, technical leadership, and strategic business management. His journey through pivotal roles from chip design to fabrication is marked by a profound depth in SoC chip design, EDA/IP, and foundry design services. As a gifted Program Manager, Gordon excels in steering complex projects amid tumultuous environments, solving critical risks, and fostering cross-functional team synergies.

Currently, as the VP of Design Service at ICSprout, he is spearheading innovative solutions in foundry design service. Prior to joining ICSprout, Served as executive positions at Sien (Qingdao) and GAT for business development and was instrumental in the 40nm CMOS technology transfer from a leading overseas semiconductor company. Gordon began his career in Silicon Valley, where he honed his skills in engineering and program management at eminent organizations such as Synopsys and Marvell, alongside other notable semiconductor firms. In 2002, Gordon embarked on a groundbreaking move by joining SMIC (Shanghai) and successfully initiated a design service team. Gordon received MSEE degree from Florida Institute of Technology

Abstract: EDA plays a crucial role in the semiconductor industry by enabling the creation of semiconductor chips through virtual simulation of silicon wafers. To bridge the gap between virtual design and actual manufacturing, foundry process engineers leverage device-driven EDA tools like TCAD to simulate semiconductor manufacturing processes and device operations. On the other hand, design-driven EDA tools such as the Spice model translate silicon behavior into electrical parameters for chip designers to simulate. However, a gap often exists between virtual simulation results and actual silicon wafers.

One innovative approach to address this gap is to utilize AI to build virtual manufacturing models, which leverage big data from both manufacturing process characteristics and design electrical properties. ICSprout, the world's only university-operated 12-inch wafer fab, has amassed a substantial amount of silicon data since its inception in 2022. This data, encompassing CMOS, eFlash, BCD, and other technologies, has facilitated the development of an AI virtual manufacturing model for individual process steps such as CESL, Thin Film Deposition, Oxidation, and CMP.

This paper presents the progress of an AI model for a single process step, CESL. Using approximately 16K sets of design and process silicon data from the ICSprout fab environment, an AI model was trained to predict process parameters based on the required electrical properties of the chip design. The developed AI model achieves highly accurate CESL process estimation with 97% accuracy. Notably, the prediction is bidirectional, enabling the model to provide precise electrical performance prediction given process combination inputs.

This model offers significant benefits to both designers and manufacturers, with the potential to reduce R&D costs and Design of Experiments (DOE) cycle time.

14:00-14:20 | Paper ID: 34 | Guangxi Fan, Shanghai Jiao Tong University

Speech Title: Fast Design Technology Co-Optimization Framework for Emerging Technology with Hierarchical Graph Embedding

Author(s): Tianliang Ma, Guangxi Fan, Xuguang Sun, Zhihui Deng, Kainlu Low, Leilai Shao

Abstract: In the rapidly evolving landscape of semiconductor technology, the advent of novel materials and sophisticated device architectures offers both opportunities and challenges for researchers. Efficient optimization of power, performance, and area (PPA) is essential in order to fully take advantages of emerging materials and new device structures. To address aforementioned issues, this paper presents a novel fast system technology co-optimization (STCO) framework for emerging flexible technologies. Simulation results demonstrate the advancement of our fast STCO framework with over 100X speedup in both TCAD simulation and cell library characterization comparing to commercial tools. For a comprehensive STCO iteration, covering TCAD simulation, modeling, cell library characterization and PPA evaluations, our framework achieves a runtime speedup between 1.9X to 14.1X depending on the scale of the evaluated circuits. The fast STCO framework incorporates a graph neural network (GNN)-based TCAD surrogate model, a unified compact model, and a GNN-based cell library characterization model. The developed STCO framework not only supports emerging technologies but can be applied to optimize the traditional silicon designs in advanced technology node.

14:20-14:50 | Invited Talk | Hrachya Astsatryan, National Academy of Sciences of Armenia

Speech Title: Exploring Memory Optimization: Research on Resource Management

Invited Speaker's Bio: Dr. Astsatryan is an accomplished computer scientist with a Ph.D. in Computer Science from the Institute for Informatics and Automation Problems (IIAP) and an M.S. in Applied Mathematics from Yerevan State University, Armenia. He is also a Habilitation recipient from the Institut National Polytechnique de Toulouse, France, where he defended his research on "Service Tradeoff for HPC and Big Data Infrastructures" in 2020. Dr. Astsatryan has held several fellowships, including a doctoral fellowship at the KFKI Research Institute for Particle and Nuclear Physics, Budapest, Hungary (2005-2006) and a postdoctoral fellowship at the Institute de Recherche en Informatique de Toulouse, Toulouse, France (2006-2007). His research interests span several areas, including high-performance and scientific computing, high-performance data analytics, data management and open data, and large-scale energy-aware distributed systems. Dr. Astsatryan has published over 90 articles in various prestigious journals, conferences, and workshops, and his research has been sponsored by several entities, including EC Framework Programmes, ISTC, INTAS, SNCF, and CRDF. In 2005, he was awarded by the President of the Republic of Armenia for his outstanding work in Technical Sciences and Information Technologies.

Abstract: This research delves deep into memory optimization, focusing on innovative resource management strategies in computing environments. By exploring state-of-the-art technologies such as Remote Direct Memory Access (RDMA), Compute Express Link (CXL), and disaggregated memory architectures, we aim to unravel the intricacies surrounding memory mutualization systems. Through rigorous investigation and analysis, our study sheds light on novel approaches to enhance memory efficiency, scalability, and performance.

14:50-15:10 | Paper ID: 127 | Yuan Lei, Hong Kong Applied Science and Technology Research Institute

Speech Title: Automatic Standard Cell Layout Generator Integrated with Design Expertise

Author(s): Yuan Lei, Chenyue Ma, Beiping Yan

Abstract: Standard cell library plays a crucial role in the efficient and reliable design of integrated circuits, but layout design of standard cell library remains challenging in industry today due to the complex design and time-to-market constraint. In this work, an automatic standard cell layout generator integrated with design expertise is presented. Existing layout experience is extracted and utilized for device placement. Additionally, to solve the multiple constraints for standard cell routing, an expertise-driven hybrid routing algorithm is developed and illustrated. Experimental results show that proposed layout generator can produce competitive standard cell layouts with quality comparable to expert's design from industry.

15:10-15:30 | Paper ID: 21 | Xiaohan Gao, Peking University

Speech Title: Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation

Author(s): Xiaohan Gao, Haoyi Zhang, Zhu Pan, Yibo Lin, Runsheng Wang, Ru Huang

Abstract: Standard cells are critical primitives of modern integrated circuits. Designing standard cells requires time-consuming manual optimization. Within a standard cell library, designers resize standard cells with the same functionality for different drive strengths. Building up all the layouts of all drive strengths from scratch introduces a lot of repetitive and redundant work, especially in routing. We propose a standard cell resizing framework to migrate a layout to another drive strength by imitating the routing of the existing layout. Experimental results demonstrate that our framework is capable of synthesizing layouts with competitive performance with the manual layouts on an industrial standard cell library.

TECHNICAL SESSION

TS12. Pushing the Envelope in Physical Implementation

Chair: Hailong Yao, University of Science and Technology Beijing

Time	13:30-15:10 | May 12, 2024	Venue	2-1 / Xianyang Hall

TAIK DETAILS

13:30-13:50 | Paper ID: 30 | Hailiang Li, Hong Kong Applied Science and Technology Research Institute

Speech Title: A Lightweight Inception Boosted U-Net Neural Network for Routability Prediction

Author(s): Hailiang Li, Yan Huo, Yan Wang, Xu Yang, Miaohui Hao, Xiao Wang

Abstract: As the modern CPU, GPU, and NPU chip's design complexity and transistor counts keep increasing, and with the relentless shrinking of semiconductor technology node to nearly 1 nanometer, the placement and routing have gradually become the two most pivotal processes in modern very-large-scale-integrated (VLSI) circuit back-end design. How to evaluate routability efficiently and accurately in advance (at the placement and global routing stages) has grown into a crucial research area in the field of artificial intelligence (AI) assisted electronic design automation (EDA). In this paper, we propose a novel U-Net variant model boosted by an Inception embedded module to predict Routing Congestion (RC) and Design Rule Checking (DRC) hotspots. Experimental results on the recently published CircuitNet dataset benchmark show that our proposed method achieves up to 5% (RC) and 20% (DRC) rate reduction in terms of Avg-NRMSE (Average Normalized Root Mean Square Error) compared to the classic architecture. Furthermore, our approach consistently outperforms the prior model on the SSIM (Structural Similarity Index Measure) metric.

13:50-14:10 | Paper ID: 18 | Xinfei Guo, Shanghai Jiao Tong University

Speech Title: Navigating the Shift Left Paradigm from Logic Synthesis Through Macro Placement to Signoff

Author(s): Xinfei Guo

Abstract: The shift left paradigm in Electronic Design Automation (EDA) presents a pathway for the creation of digital twins, facilitating the transition of subsequent physically-aware design processes into virtual environments. This shift empowers designers to establish stronger correlations and optimize their designs more effectively. However, it is crucial to identify when and how to implement this shift, especially considering the challenges in replicating subsequent behaviors accurately. Given that synthesis marks the initiation of the entire physical implementation phase, macro placement serves as the starting point for intensive automated placement, and timing signoff acts as a starting point for the engineering change order (ECO) process. We have pinpointed opportunities to introduce shift left updates to these critical stages. By incorporating a physically aware timing model into logic synthesis, we have significantly enhanced design quality in terms of timing. By preemptively considering macro-cell connections as a co-optimization target, improvements have been observed in routing length and congestion, leading to more efficient designs. Additionally, by closely coupling a fast and accurate timing estimation model with the following ECO process, faster timing closure has been achieved.

14:10-14:30 | Paper ID: 35 | Zhongdong Qi, Xidian University

Speech Title: Effective Heterogeneous Graph Neural Network for Routing Congestion Prediction

Author(s): Zhongdong Qi, Qi Peng, Shizhe Hu, Hailong You

Abstract: Accurate prediction of routing congestion in the placement stage is critical in digital integrated circuit design. We propose an effective heterogeneous graph neural network named HeteroNet with an encoder-decoder structure, to predict global routing congestion from placement results. General heterogeneous graphs are constructed to flexibly represent layout objects and relations between them. We also propose efficient transfer learning technique on HeteroNet. Experimental results show that HeteroNet models achieve higher

predictive performance compared to prior work. When having a network modeling one global router, the training of a new network modeling another global router can be achieved in only 17% of runtime using transfer learning, compared to training from scratch.

14:30-14:50 | Paper ID: 87 | Qingsheng Qiu, Southeast University

Speech Title: Edge Pair-Based Layout Pattern Matching Using Space-filling Curve

Author(s): Qingsheng Qiu, Yuqing Zhang, Wuxin Ge, Chao Wang

Abstract: DRC-based layout pattern matching is currently the mainstream method in the industry. However, as process nodes shrink and pattern complexity grows, the runtime of DRC-based layout pattern matching methods has increased significantly. The DRC method relies on weakly constrained one-dimensional rule checks, resulting in numerous potential matching regions. In addition, it is difficult to accurately describe patterns with DRC rules, which leads to a complex matching verification process. To address the above issues, we propose a novel edge pair-based approach that reduces the number of potential matching regions while speeding up the search process. Additionally, we employ a hash method for simplified and effective matching verification. Furthermore, as the hash method relies on spatial indexing, we utilize space-filling curves to accelerate index construction and reduce region query time. Experimental results show that compared to the state-of-the-art pattern matching method, our proposed approach achieves a speedup ranging from 5.6× to 17.3× with 100% accuracy.

14:50-15:10 | Paper ID: 124 | Zun Xue, Southeast University

Speech Title: Aging-aware Logic Restructure Acceleration based on Heterogeneous Graph Learning

Author(s): Zun Xue, Yuchen Liu, Yuyang Ye, Tinghuan Chen, Hao Yan, Longxing Shi

Abstract: Aging effects such as NBTI, introduce new challenges to circuit design. As NBTI is heavily related to the workload features of the circuit, logic restructuring techniques are proposed to modify the signal probability of internal nodes in a circuit to reduce timing degradation. However, decreasing signal probability does not guarantee aging-aware timing improvement, since the new structure will lead to a different implementation with unexpected delay characteristics. Thus, selecting candidates for timing optimization presents a challenge during logic restructuring. In this work, we define the question as an anomaly detection problem. Critical paths of the netlist are represented with heterogeneous graphs to accurately capture the connectivity of complex logic gates. An HGAT-based autoencoder model is then deployed to learn and obtain valid candidates for a predefined logic restructure technique. The result shows improved runtime and result quality compared with traditional heuristic-based algorithms, confirming the efficacy of our proposed model.

TECHNICAL SESSION

TS13. Design, Safety and Reliability

Chair: Jiliang Zhang, Hunan University

Time	13:30-15:10 | May 12, 2024	Venue	2-6 / Baoji Hall

TAIK DETAILS

13:30-13:50 | Paper ID: 169 | Binyu Yin, Sun Yat-sen University

Speech Title: Electromigration Based Hardware Trojan Defense in Integrated Circuit

Author(s): Binyu Yin, Linlin Cai, Haoyu Zhang, Wangyong Chen

Abstract: Recently, Hardware Trojans are gaining increasing attention due to their ability to cause damage to critical circuits through covert attack methods, which poses significant threats to electronic systems. Among the various attack methods of Hardware Trojans, those based on electromigration (EM) induced circuit aging are particularly feasible. In this paper, we investigate Hardware Trojan defense in integrated circuits based on an advanced three-dimensional physical electromigration model. By extracting characteristic structures from specific circuits, we conduct the electromigration failure analysis and propose Hardware Trojan defense strategy based on specific interconnect structures. Through these works, we demonstrate the vulnerable attacking locations of different interconnect structures and provide the guidance for electromigration based Hardware Trojans defense in IC design.

13:50-14:10 | Paper ID: 68 | Zhangyu Li, National University of Defense Technology

Speech Title: Towards Evaluating SEU Type Soft Error Effects with Graph Attention Network

Author(s): Zhangyu Li, Tun Li, Chang Liu, Liang Wang, Chunxue Liu, Yang Guo, Wanxia Qu

Abstract: With the rapid development of integrated circuit manufacturing processes, soft errors have emerged as a pivotal factor that influences circuit reliability. This paper endeavors to investigate the rapid estimation of the impact of the single event upset (SEU) on the logic behaviors of flip-flops in a circuit using machine learning methods. A major challenge currently faced when applying machine learning methods for SEU evaluation is the absence of publicly available circuit datasets. Therefore, this paper employs the fault injection method to acquire circuit data such as soft error sensitivity. Subsequently, it models the gate-level netlist and integrates the netlist models with the acquired data to construct a dataset. Finally, a model based on graph attention network (GAT) is developed and we use the leave-one-out cross validation method to evaluate the performance. Compared to neural network methods skilled at handling structured data, the experimental results indicate that the method proposed in this paper has better predictive performance. It achieves an average absolute error of 0.064, representing a 43.46% improvement over the baseline.

14:10-14:30 | Paper ID: 78 | Na Bai, Anhui University

Speech Title: A High Critical Charge 16T Soft-Error-Aware SRAM for Aerospace Applications

Author(s): Na Bai, Wenhao Zhu, Xinjie Zhou, Yaohua Xu, Yi Wang

Abstract: This paper proposes an inside-aware-soft-error 16T (IASE16T) SRAM unit for aerospace applications to address single-event upsets (SEUs) caused by high-energy particles in space. It outperforms other soft error-aware SRAM units (SARP12T, LWS14T, SAR14T, RSP14T, S8P8N16T, EDP12T, SIS10T) by fully recovering from SEUs and exhibiting a critical charge exceeding 105fc, superior stability, and write latency time. Compared to alternatives, IASE16T demonstrates significantly improved hold static noise margin (HSNM) (by approximately 60%-138%). However, its read speed is slightly reduced due to having only one discharge path, and it incurs some area loss due to its 16T structure.

14:30-14:50 | Paper ID: 102 | Xi Tian, National University of Defense Technology

Speech Title: CPGPUSim: A Multi-dimensional Parallel Acceleration Framework for RTL Simulation

Author(s): Xi Tian, Cheng Yue, Yan Pi, Tun Li, Wanxia Qu

Abstract: Parallelism capability of GPUs makes accelerated RTL simulation possible by utilizing structure-level and data-level parallelism of designs. However, due to the existence of feedback loops in circuits, how to achieve data-level parallelism in a single testbench is still a great challenge. In this paper, we propose a novel CPGPU-accelerated RTL simulation framework with loop unrolling techniques to utilize data-level parallelism for RTL simulation acceleration. In the framework, designs under simulation are first processed by loop unrolling. Then the processed designs are partitioned and the simulation task of each partition is assigned to be simulated on CPU or GPU according to its characteristics. The design partitioning method makes full use of the parallel capabilities of RTL simulation using GPU. The promising experimental results show that the proposed CPGPU-accelerated RTL simulation achieves up to 32.2x speed-up than ESSENT and 4.8x speed-up than traditional GPU-based acceleration methods.

14:50-15:10 | Paper ID: 183 | Mingbo Hao, Southeast University

Speech Title: OhmNet: General Static IR Drop Estimation Neural Network Architecture

Author(s): Mingbo Hao, Junyi Qian, Zhiting Li, Zhangrui Qian, Weiwei Shan

Abstract: Static IR drop analysis is a crucial part in the signoff stage of the IC design flow. Conventional commercial tools are often time-consuming, hindering the acceleration of the industrial design cycle. We propose a novel OhmNet neural network architecture to provide quick and accurate predictions for the limited IR drop mitigation time budget in the IC design period. OhmNet incorporates circuit constraint into the model optimization process. This approach not only facilitates the convergence of the model but also enhances its interpretability. Furthermore, the implementation of the OhmNet architecture is modular. We developed four configurable modules that can be customized to meet specific accuracy or speed requirements, leading to the creation of the OhmNet-23 network. The experimental results show that the network is still sensitive to isolated, small-scale regions with high IR drop. Compared with the ground truth, the average correlation coefficient (CC) and the mean absolute error (MAE) of the estimation result are 92.92% and 2.14 mV, respectively, and the estimation speed is 28.98% faster than the method based on U-Net.

TECHNICAL SESSION

TS14. Synthesis Techniques: The Next Generation

Chair: Qiang Xu, The Chinese University of Hong Kong

Time	13:30-15:20 | May 12, 2024	Venue	2-5 / Weinan Hall

TAIK DETAILS

13:30-14:00 | Invited Talk | Yun Shao, Shenzhen Giga Design Automation Co., Ltd.

Speech Title: Synthesis Technology for Commercial Tools

Invited Speaker's Bio: Dr. Shao, Yun received his B.S. degree in Wireless Communication from Southeast University, Nanjing, China, in 1995. He got his Ph.D. degree in Electrical and Computer Engineering from University of Iowa, USA, in 2002. Dr. Shao has been working in EDA industry for more than 20 years. He held senior positions in R&D engineering at Synopsys and made important contributions to Design Ware, Design Compiler and Fusion Compiler. Currently, he is a senior R&D director in Giga Design Automation, in charge of developing advanced synthesis technology.

Abstract: Advanced digital designs are getting more complex and challenging in the last two decades. This trend drives commercial synthesis tools to improve on many aspects. This talk will review some key features of RocSyn and its related technologies. Furthermore, reference methodology will be presented to achieve best PPA and turnaround time.

14:00-14:20 | Paper ID: 213 | Xing Li, Huawei Noah's Ark Lab

Speech Title: A General Framework for Efficient Logic Synthesis

Author(s): Lei Chen, Xing Li, Tsaras Dimitrios, Zhihai Wang, Yinqi Bai, Mingxuan Yuan

Abstract: Logic synthesis synthesize circuit structures to optimize specific targets given reasonable constraints and runtime, utilizing a set of well-defined operators. Most existing synthesis operators are designed heuristically with a general paradigm of traversing circuit cuts or sub-graphs and making local replacements, when certain transformations offer synthesis gains. These transformations are usually obtained via invoking certain synthesis engines and can be time-consuming. However, most of these computations are redundant and lead to no further replacements. The efficiency of these operators is crucial for improving runtime and optimization convergence. Therefore, we propose a general framework for efficient logic synthesis that prunes unnecessary logic transformation and gain measurements, while maintaining synthesis effectiveness. To address the diverse needs of different operators, considering factors such as model inference time, ease of deployment, and interpretability, we propose several methods tailored to specific scenarios and unify them into a general framework. The framework is validated through experiments on both public and industrial circuits. For example, the expertise based scoring method can accelerate drw by about 35% with negligible effectiveness loss, and a GNN-basedmethod achieves up to 3.1x faster runtime of mfs2.

14:20-14:40 | Paper ID: 114 | Liwei Ni, Peng Cheng Laboratory

Speech Title: Enhancing ASIC Technology Mapping via Parallel Supergate Computing

Author(s): Ye Cai, Zonglin Yang, Liwei Ni, Biwei Xie, Xingquan Li

Abstract: With the development of large-scale integrated circuits, electronic design automation~(EDA) tools are increasingly emphasizing efficiency, with parallel algorithms becoming a trend. The optimization of delay reduction is a crucial factor for ASIC technology mapping, and supergate technology proves to be an effective method for achieving this in EDA tools flow. However, we have observed that increasing the number of generated supergates can reduce delay, but this comes at the cost of an exponential increase in computation time. In this paper, we propose a parallel supergate computing method that addresses the tradeoff between time-consuming

and delay optimization. The proposed method utilizes the input-constrained supergate pattern to parallelly generate the supergate candidates, and then filter the valid supergates as the results. Experiment results show the efficiency of the proposed method, for example, it can attain the improvement of 4 times speedup in computation time and 10.1 in delay reduction with 32 threads.

14:40-15:00 | Paper ID: 85 | Ming Yan, Ningbo University

Speech Title: Exact Synthesis and Inversion Optimization for 3-input Resistive Majority Based Logic-in-Memory

Author(s): Ming Yan, Guanghai Dong, Yong Xiao, Yun Shao, Zhufei Chu

Abstract: Resistive random access memories (RRAMs) serve as compact non-volatile storage devices capable of storing data and performing Boolean operations. They inherently support 3-input Resistive Majority (RM3) logic operations, making them integral to in-memory computing applications. Prior methods have adapted general-purpose logic networks for RM3 logic. This paper introduces RM3-inverter graphs (RM3IGs) as dedicated logic representations, employing RM3 and inverters as primitives.We utilize an exact synthesis algorithm to derive optimal RM3IG implementations for 4-input Boolean functions to establish a database. Then, leveraging a logic restructuring algorithm and the database, we derive initial RM3IG structures. Furthermore,we propose a heuristic algorithm for inversion optimization within RM3IGs. Our experimental results show a reduction in the number of nodes and inverters, demonstrating a 14.0% reduction in size and a 17.7% reduction in level compared to previous approaches.

15:00-15:20 | Paper ID: 132 | Xiangli Chen, Nanjing University of Aeronautics and Astronautics

Speech Title: A Topology-flattening-based Automated Incremental Synthesis Method

Author(s): Xiangli Chen, Gang Chen

Abstract: As chip development enters the “post-Moore's Law era,” the core driving force behind chip design will gradually shift from enhancements in performance power and area (PPA) consumption to building autonomous chips for emerging applications. However, bridging the gap between domain-specific systems and traditional chip design complicates the process, posing challenges for iterative chip development. Logic synthesis, as a tedious and time-consuming step at the front end of the process, stands as one of the major bottlenecks in accelerating chip iterative development. To address this, we propose a topology-flattening-based automated incremental logic synthesis method. It divides projects into functional blocks, allowing for selective re-synthesis of modified parts, significantly improving iteration efficiency. Building upon this technique, we have developed an automated synthesis system capable of flexibly integrating existing open-source synthesis tools to achieve automated incremental synthesis. Experimental testing conducted on the open-source synthesis tool Yosys demonstrates that our proposed method enhances the iteration efficiency of chip design front-end, providing an effective solution for automated incremental synthesis.

TECHNICAL SESSION

TS15. Chiplet and 3DIC Revolution & High-Level Synthesis Frontier

Chair: Yun Liang, Peking University

Time	13:30-15:20 | May 12, 2024	Venue	2-9 / Presidium Room

TAIK DETAILS

13:30-14:00 | Invited Talk | Pei-Hsin Ho, Shanghai UniVista Industrial Software Group Co., Ltd.

Speech Title: Chiplet Explorer: Optimizing ICs with Diverse Chiplets Through Automated Solution-space Exploration

Invited Speaker's Bio: Dr. Pei-Hsin Ho serves as the Chief Technology Officer (CTO) of UniVista Industrial Software Group, where he oversees R&D of emulation and digital implementation. Prior to his current role, Dr. Ho held the position of Synopsys Fellow, where he led research and development teams of Synopsys Emulation, Physical Design, and Formal Verification products. He has also contributed significantly to the field of Formal Verification during his tenure at Intel Strategic CAD Labs. Dr. Ho holds 12 U.S. patents and authored over 30 peer-reviewed papers with 10,000+ citations (based on Google Scholar). He received the Best Paper Award at DAC in 1999 and candidacy for the Best Paper Award at DAC in 2009.

Abstract: The integration of multiple heterogeneous chiplets presents opportunities to enhance both cost-efficiency and performance of ICs. However, this approach also brings forth challenges such as performance optimization, energy efficiency, signal and power integrity, thermal management, and Design for Test (DFT) considerations. In this talk, we will discuss the four critical dimensions of the solution space of implementing an IC using multiple heterogenous chiplets and discuss an innovative methodology of Chiplet Design Automation, leveraging EDA tools and IPs, to enable the designer to explore a much broader solution space and thus discover a much better solution utilizing diverse chiplets.

14:00-14:20 | Paper ID: 83 | Renjing Hou, Beijing University of Posts and Telecommunications

Speech Title: Array Partitioning Method for Streaming Dataflow Optimization in High-level Synthesis

Author(s): Renjing Hou, Jianwang Zhai, Yajun Wang, Zhe Lin, Kang Zhao

Abstract: High-level synthesis (HLS) is a popular method that allows designers to describe the behavior-level functionality and automatically generates efficient register-transfer level (RTL) descriptions. In HLS, dataflow is the key micro-architecture to achieve high parallelism. However, the streaming dataflow is often limited by its strict conditions such as sequential access on the potential channels. To settle this issue, this paper proposes an efficient array partitioning method for the streaming dataflow inference. The key is to explore the potential array partitioning mode which matches the sequential access requirements by streaming channels. An experimental case study is presented on the inference of the convolutional neural networks (CNN).It indicates that the proposed method can achieve about 28.6% performance improvements compared with the default dataflow,with the cost of 7.2% power increasement.

14:20-14:40 | Paper ID: 74 | Chen Yang, Beijing University of Posts and Telecommunications

Speech Title: Automated Python-to-RTL Transformation and Optimization for Neural Network Acceleration

Author(s): Chen Yang, Renjing Hou, Qirui Yang, Wenjian Yu, Kang Zhao

Abstract: In order to optimize the process of accelerating large-scale neural network (NN) on field-programmable gate array (FPGA), this paper presents and optimizes the automatic flow based on HeteroCL and Xilinx Vitis HLS. This flow could transform python-based NN description to Verilog RTL running on FPGA. To improve its quality of result (QoR), many key optimization methods are proposed for the high-level synthesis

(HLS) input, including fixed-point quantization, loop pipelining, convolutional buffer and others. To prove the feasibility of proposed optimization techniques, the convolutional NN (CNN) is selected as the experimental case study. And the results show that the delay and power consumption due to optimization techniques are significantly reduced.

14:40-15:00 | Paper ID: 63 | Wenbo Guan, Xidian University

Speech Title: An Equivalent Circuit Model for Elliptic Cylindrical TSV Considering the Temperature Influence

Author(s): Wenbo Guan, Xiaoyan Tang, Hongliang Lv, Jingru Tan, Yuming Zhang, Yimen Zhang

Abstract: Through Silicon Via (TSV) technology is a key technology to realize multi-layer chips and its structure and equivalent circuit model have attracted much attention. With the continuous reduction of chip size, higher requirements are put forward for the equivalent circuit model of TSV. Elliptic cylindrical TSV has the advantages of small occupation area and good transmission characteristics. The established TSV model takes into account factors such as capacitance changes caused by non-uniform diameters. Under the temperature effect, the equivalent circuit model of elliptic cylindrical TSV is established, and then its RLCG parasitic parameters are extracted. By comparing the S parameter simulation results of HFSS and ADS, the accuracy of the equivalent circuit is verified. It is indicated that the circuit model of the novel elliptic cylindrical TSV can well predict the S parameters of the TSV in 0~50GHz.

15:00-15:20 | Paper ID: 205 | Siyuan Xu, Huawei Noah's Ark Lab

Speech Title: Cross-die Optimization For Logic-on-Memory Face-to-Face Bonding 3-D IC Designs

Author(s): Siyuan Xu, Hongzhong Wu, Mingxuan Yuan

Abstract: The Moore's laws are pushing chips to grow smaller and higher in density. On the other hand, vertical chip stacking (i.e: three-dimensional integration or package) has attracted both academia and industry as it can lead to shorter wire interconnection, lower power consumption, and higher efficiency. However, this poses a significant challenge for cross-die co-optimization. In this paper, we discuss the cross-die optimization of 3D logic-on-memory integration. The background issues will be presented firstly and following by some of the recent work. Finally related difficulty including netlist partitioning, netlist representation, cross-die optimization, and its estimation and simulation will be discussed.

TECHNICAL SESSION

TS16. Memory Testing and Yield Enhancement

Chair: Fan Yang, GWX Technology

Time	16:00-18:10 | May 12, 2024	Venue	2-9 / Presidium Room

TAIK DETAILS

16:00-16:30 | Invited Talk | Xin Li, Duke Kunshan University

Speech Title: Robust Wafer Classification with Imperfectly Labeled Data

Invited Speaker's Bio: Xin Li received the Ph.D. degree in Electrical & Computer Engineering from Carnegie Mellon University in 2005. He is currently a Professor in ECE at Duke Kunshan University and serves as the Associate Vice-Chancellor for Graduate Studies and Research. His research interests include integrated circuits, signal processing and data analytics. Dr. Li was the Deputy Editor-in-Chief of IEEE TCAD. He was an Associate Editor of IEEE TCAD, IEEE TBME, ACM TODAES, IEEE D&T and IET CPS. He was the General Chair of ISVLSI and FAC. He received the NSF CAREER Award in 2012 and six Best Paper Awards from IEEE TCAD, DAC, ICCAD and ISIC. He is a Fellow of IEEE.

Abstract: Wafer classification is a critical task for semiconductor manufacturing. Most conventional algorithms require a large-scale perfectly-labeled dataset to train accurate classifiers. In practice, it is usually difficult or even impossible to collect perfect labels without errors, and the classification accuracy in the presence of imperfectly labeled data may substantially degrade. In this presentation, we will discuss a number of novel techniques to facilitate robust wafer classification with noisy labels. These techniques can be classified into three broad categories: (1)data cleaning methods, (2) loss-function-based methods, and (3) co-teaching methods. The efficacy of robust wafer classification will be demonstrated by several industrial datasets.

16:30-16:50 | Paper ID: 165 | Rongjie Yang, Sun Yat-sen University

Speech Title: An Efficient Grouping Method for Large-Scale MBIST

Author(s): Rongjie Yang, Zheng Wang, Minghua Shen

Abstract: Memory built-in self-test (MBIST) is an important design-for-test (DFT) technique for embedded memories, and MBIST grouping is the most significant part of it. However, as the number of embedded memories increases, previous MBIST grouping methods result in long grouping time or low-quality grouping results. In this paper, we propose an efficient grouping method for large-scale MBIST. Our method combines greedy algorithm (GA) with simulated annealing algorithm (SA), reducing grouping time significantly while maintaining high-quality grouping results. Experimental results show that, compared to previous SA-based methods, our method can reduce grouping time by 43% for large-scale MBIST. It reduces the number of groups by 178 and 17 for large-scale MBIST compared to previous SA-based and GA-based methods, respectively.

16:50-17:10 | Paper ID: 193 | Yang Li, China University of Petroleum

Speech Title: EMGA: An Evolutionary Memory Grouping Algorithm for MBIST

Author(s): Yang Li, Yongqiang Duan, Hao Zhang, Dan Niu, Xiao Wu, Zhou Jin

Abstract: MBIST (Memory Built-In Self-Test) is a widely used methodology in chip design and fabrication to detect and localize faults in memories. Due to the large memory sizes of modern chips, memories need to be grouped in order to manage and test them efficiently. However, due to the high number of constraints and memories, the time complexity of solving directly using heuristic algorithms is high and the grouping results obtained are of poor quality. In this paper, we propose a heuristic-based MBIST grouping algorithm to maintain high efficiency while achieving high quality grouping. We firstly divide the numerous constraints into two categories to reduce the constraint dimensions and obtain an initial grouping result. We then use a greedy algorithm with a penalty term to quickly obtain the result that satisfies all the constraints from the initial result in order to reduce the time consumption and the size of the grouping. In order to avoid local optimal solutions,

we further use an improved genetic algorithm to optimize the result of the greedy algorithm to obtain higher quality groupings. The experimental results demonstrate that our algorithm reduces the number of groups 119.44% on average compared with the K-Means method. Compared with simulated annealing algorithm and genetic algorithm, EMGA reduces the number of groups by 8.35% and 4.66%, and time by 79.51% and 73.30%, respectively.

17:10-17:30 | Paper ID: 162 | Zhixing Liu, Xidian University

Speech Title: An Efficient Grouping Algorithm with Build-in-self-test for Multiple Memories

Author(s): Zhixing Liu, Jielin Xu, Jing Tang, Song Yang, Hailong You

Abstract: With the advancement of manufacturing processes and the ever-increasing demand for system-on-chip (SoC) computations, modern SoCs integrate a myriad of embedded memories, posing significant challenges for memory unit testing. Presently, the Memory Built-in Self Test (MBIST) method is often used by industry to effectively test memories. However, the burgeoning quantity of memories entails substantial resource waste when allocating test logic for each memory unit. It is imperative that the auxiliary circuitry for testing purposes remain minimal while fulfilling the testing requisites. Rational grouping of memories to share Built-In Self-Test (BIST) logic to mitigate unnecessary overhead during testing emerges as a plausible research problem. In this paper, we propose an efficient three-step partitioning approach for shared memory BIST logic, focusing on grouping rules and variable constraints. This methodology is applicable to diverse memory types and BIST components. With the objective of minimizing the number of memory groups while satisfying constraints, our approach aims to reduce BIST logic, thereby mitigating area overhead. Following the initial partitioning to generate compatible memory groups, a multi-threaded approach is employed for the subsequent partitioning of all memory groups. By representing memories that satisfy distance constraints as graphs and substituting the greedy algorithm with the BronKerBosh algorithm, superior solutions are attained. Experimental results indicate an average improvement of 9% in solution quality compared to the greedy algorithm.

17:30-17:50 | Paper ID: 128 | Zhongxi Guo, Southeast University

Speech Title: An Efficient SRAM Yield Analysis Method Using Multi-Fidelity Neural Network

Author(s): Zhongxi Guo, Weihan Sun, Ziqi Wang, Yihui Cai, Longxing Shi

Abstract: As microelectronic fabrication technology advances rapidly, the yield of static random access memory (SRAM) blocks has to be guaranteed at a high level due to the large number of replicated cells. Accurate and efficient yield analysis methods are in great demand to reduce manufacturing costs induced by process variations. In this article, we integrate multi-fidelity (MF) neural networks as surrogate models into the importance sampling (IS) method, which expedites the search process for optimal shift vectors (OSV). Compared to the conventional OSV searching methods, the proposed method significantly reduces the number of simulations required for model training while maintaining accuracy. Finally, the failure rates are estimated using IS process until convergence. The experimental results on the 64-bit SRAM column show that preserves the advantages of IS-based methods, achieving up to 2.1$\times$ to 14.3$\times$ the efficiency and accuracy compared to the state-of-the-art methods for high-dimensional circuits.

17:50-18:10 | Paper ID: 111 | Haixiang Qiu, Semitronix Corporation

Speech Title: RLIF-Net: Unsupervised Trace-SPC Fault Detection Solution Based on Representation Learning and Isolation Forest

Author(s): Haixiang Qiu, Hui Jiang

Abstract: Wafer manufacturing is a complex process involving hundreds of process steps. Detecting and identifying potential anomalies and malfunctions in sensor parameters are crucial for improving production yield. However, traditional rule-based or statistical methods fail to meet the requirements of accuracy and efficiency. To address this issue, we propose an innovative model called RLIF-Net that combines deep learning with Isolation Forest. The deep learning module is used to extract multi-dimensional feature vectors at each timestamp, while the Isolation Forest module takes the multi-dimensional feature vectors at each timestamp as input for anomaly detection in the timestamp dimension. We conducted experiments using a real industrial dataset and compared our model with several state-of-the-art models. The results demonstrate that our model exhibits strong learning and representation capabilities, enabling it to learn from large amounts of data and identify complex anomaly patterns.

TECHNICAL SESSION

TS17. EDA Strategies for FPGA Deployment

Chair: Jun Liu, X-EPIC

Time	16:00-18:20 | May 12, 2024	Venue	3-6 /Yulin Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Hailong You, Xidian University

Speech Title: An Efficient Multi-FPGA System-Aware Hypergraph Partitioning Framework

Invited Speaker's Bio: Dr. You Hailong is a Professor with Xidian University, received the B.Eng. degree in optoelectronic technology and the Ph.D. degree in microelectronics from Xidian University, Xi'an, China, in 2002 and 2006, respectively. His current research interests are emulation and prototyping, Design for Reliability. and microelectronics reliability. Dr. You's research record includes more than 60 articles in academic journals and international conferences such as DATE, JEDS, TODAES, Integration, ASP-DAC, Microelectronics Reliability, etc., three textbooks on microelectronics reliability., more than 10 awarded patents.

Abstract: Nowadays, multi-FPGA systems (MFS) are widely used in logic emulation and rapid prototyping of large designs. These systems emerged as the primary solution because of their high flexibility and cost-effectiveness. A multi-FPGA system consists of several FPGAs connected by physical wires or a programmable interconnection network. However, FPGAs are usually not fully connected because of limited I/O resources. The connections between different FPGAs could be irregular. Therefore, if an inter-FPGA signal starts from one FPGA and heads for another FPGA that is not directly connected to the source one, this would introduce the hops and increase the delay. Furthermore, the time-division multiplexing (TDM) technique is commonly used in multi-FPGA systems to allow multiple signals sharing the same TDM only to occupy one wire, increasing signal latency costs. Therefore, the hops and the TDM will cause longer delays in the signal path and further decrease system performance.

In the typical compilation flow of a multi-FPGA system, partitioning, and system-level routing are performed in the early stages. These two processes involve dividing a large circuit into smaller sub-circuits and interconnecting the FPGAs. As circuit design becomes increasingly large and sophisticated, these steps play an increasingly critical role in system performance and delay. There exist several related works that focus on partitioning and system-level routing; for example, hMETIS in 1997, PaToH in 2011, KaHyPar in 2017, and SpecPart in 2022 are all presented to address the cut-size issue. However, a multi-FPGA system introduces additional FPGA topology constraints and complex optimization objectives such as hop and TDM, which present more significant challenges in solving these problems.

This report introduces the MaPart, a novel hypergraph partitioning framework that aims to minimize the maximum path delay in a multi-FPGA system. In MaPart, the core engine, TopoPart+, which employs the improved multi-level partitioning paradigm and the very fast candidate FPGA propagation theorem and corollary, strives to achieve a non-hop partition. When obtaining a non-hop partition is unfeasible, MaPart combines binary search with TopoPart+ to minimize the maximum hop count during partitioning. Furthermore, TopoPart+ incorporates two successive local refinement algorithms that optimize the TDM ratio, reduce total hop count, and alleviate congestion on critical paths. In the system-level routing stage, MaPart integrates a system-level router based on layered graphs, enabling flexible control of the hop count based on the timing criticality of each path.

In industry and large-scale design experiments, TopoPart+ provides enhanced problem-solving capabilities and achieves a remarkable 96% reduction in cut-size compared to the baseline. In overall performance comparison to the SOTA algorithm, the MaPart achieves a significant 37% reduction in delay.

16:30-17:00 | Invited Talk | Jing Zhou, Beijing Microelectronics Technology Institute

Speech Title: A Security-Driven FPGA Application Development Workflow Based on GCN Algorithm

Author(s): Ke Xiao, Lei Chen, Yanlong Zhang, Shuo Wang, Jing Zhou, Xueting Zhang, Shuang Jiang

Invited Speaker's Bio: Jing Zhou is currently a senior engineer at Beijing Microelectronics Technology Institute. She has published over 20 papers in peer-reviewed journals and conferences and six patents. She has undertaken and participated in a number of national or ministerial key scientific research projects. Her research interests include FPGA EDA algorithm, high-reliability FPGA software design technology, hardware security, hardware Trojan detection and defense technology.

Abstract: As the complexity of integrated circuit designs increases and the supply chain becomes more globalized, the threat of hardware Trojans has escalated, posing higher security requirements for Electronic Design Automation (EDA) software.This study introduces an FPGA integrated development environment and FPGA application development process that incorporates a hardware Trojan detection algorithm. It extracts features from the netlist after FPGA synthesis and utilizes Graph Convolutional Networks (GCN) to process the rich structural features in the netlist. To address the issue of imbalanced datasets,we incorporate the GraphSMOTE technique to enhance the model's generalization capability by synthesizing minority class samples. In the classification phase, an optimized GCN model is employed to determine whether each node is a Trojan node. Comparative experiments with several other models demonstrate a significant improvement in detection accuracy, achieving the highest F1 score and a high True Positive Rate (TPR), thereby validating the effectiveness and superiority of the GCN-based method in the field of hardware Trojan detection. This study not only enhances the security of the FPGA application development process but also provides new insights and tools for subsequent research in hardware security.

17:00-17:20 | Paper ID: 118 | Shang Wang, University of Alberta

Speech Title: FPGA Divide-and-Conquer Placement Using Deep Reinforcement Learning

Author(s): Shang Wang, Deepak Ranganatha Sastry Mamillapalli, Tianpei Yang, Matthew E. Taylor

Abstract: This paper introduces the problem of learning to place logic blocks in Field-Programmable Gate Arrays (FPGAs) and a preliminary learning-based method. In contrast to previous FPGA placement algorithms, we depart from heuristic search and instead employ Deep Reinforcement Learning (DRL) for the placement task with the objective of minimizing wirelength. To facilitate the agent's decision-making, we design unique state representations that include the chipboard observations and interconnections between different blocks. Additionally, we propose the decomposition training paradigm to address the nature of large search space and sparse rewards in the placement problem by dividing the full problem into small subtasks and solving each subtask using DRL respectively. Experiments demonstrate the effectiveness of the decomposition paradigm on FPGA placement tasks.

17:20-17:40 | Paper ID: 123 | Chen Wu, EagleChip Technology Limited

Speech Title: PatRouter: An Optimal-Pattern-Oriented Routability-driven Routing Algorithm for FPGA

Author(s): Chen Wu, Xuhui Li, Qiang Wang

Abstract: Quality of routing results is one of the most significant aspects for modern FPGA design. Although various attempts have been made on improving routability and runtime, the existing approaches pay little attention on the nature of PathFinder-based routers to optimize the quality of routing results. In this paper, we propose PatRouter, an optimal-patternoriented routability-driven algorithm to improve the quality of routing. A pattern generator is first developed to build optimal patterns, which is defined as routing paths with the minimal number of wire segments to represent the routing resources in device. On this basis, we propose a pattern-oriented min-segment (PoM) connection router, which intensively route connections with optimal patterns. In this way, PoM searches for routing paths under pruned routing resources, thus, also reducing runtime. Meanwhile PoM will gradually increase the number of wire segments for congested connections to maintain

routability. To further improve routability, we design a patternoriented A* (PoA) connection router to address the most congested connections by searching the whole routing resources. Experiments on our self-defined architecture and benchmarks show that PatRouter optimizes the quality of routing results while maintaining routability. To be specific, with PatRouter, 46.9% of the total connections are routed with minimal number of wire segments on average. Meanwhile, 22.2% of the total connections need sub-optimal patterns within 2 wire segments from optimal.Comparison with the latest approaches on Titan benchmark also shows 1.2× reduction in wirelength.

17:40-18:00 | Paper ID: 208 | Zhuoli Wang, Beijing Microelectronics Technology Institute

Speech Title: AIP-SEM: An Efficient ML-Boost In-Place Soft Error Mitigation Method for SRAM-based FPGA

Author(s): Zhuoli Wang, Lei Chen, Shuo Wang, Jing Zhou, Chunsheng Tian, Hanxu Feng

Abstract: With the wide application of SRAM-base FPGA in aerospace engineering, the radiation resistance performance of FPGAs becomes unprecedented important. To correct errors, the Triple Modular Redundancy (TMR) technique uses a voter and incurs significant PPA overhead. We propose an efficient in-place soft error mitigation method, that can mitigate soft errors without any additional PPA overhead. Compared to other synthesis-based algorithms, our method use an XGBoost-based prediction model which predicts time-consuming circuit metrics. For the EPFL benchmark circuit, our approach achieves up to 19.42% runtime speedup, and under 3% loss on the failure rate reduction.

18:00-18:20 | Paper ID: 140 | Chenxi Huang, Xidian University

Speech Title: System Routing and TDM Assignment Optimization in Multi-2.5D FPGA-Based Prototyping Systems

Author(s): Chenxi Huang, Pengfei Chu, Shunyang Bi, Richard Sun, Hailong You

Abstract: 2.5-D FPGA has been used in many Multi-FPGA Systems (MFS) for prototype verification due to its higher logic capacity and larger number of pins. The FPGA is composed of multiple dies connected with special wires. Due to the limited connections, FPGA-based system-level routing may cause internal congestion and lead to implementation failures. In addition, TimeDivision Multiplexing (TDM) is used in inter-FPGA connections to improve logic utilization, and each signal is assigned a TDM ratio. However, the increase in inter-FPGA delay of signals positively correlated with the ratio. And the system performance will be significantly influenced by these internal congestions and TDMs. In this paper, a system-level routing framework with hybrid initial routing and two-stage reroute algorithms that generates legal and high-quality routing results for a 2.5-D MFS is proposed. Afterwards, a three-step framework is proposed to generate legal TDM ratios and optimize the system's performance, where a high-quality discretization algorithm based on bottom-up dynamic programming is implemented to optimize the performance losses. The experimental results demonstrate an average improvement of 8% in the solution's quality compared with our baseline algorithms within reasonable runtime. And compared with the winner of the 5th EDA Elite Challenge, the quality of our solutions achieved the best results in most cases.

TECHNICAL SESSION

TS18. Emerging Horizons in TCAD

Chair: Chen Shen, Suzhou PFTN Semiconductor Co., Ltd.

Time	16:00-18:10 | May 12, 2024	Venue	3-3 / Hanzhong Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Karen Gambaryan, Yerevan State University

Speech Title: Graded Composition Double Quantum Dots: Nucleation Features, Characterization and Application for New Generation Nano-Optoelectronic Devices

Invited Speaker's Bio: Professor Karen Gambaryan has completed his PhD thesis in 1988 at Yerevan State University (YSU). He has defended the second doctorate dissertation (habilitation) and received Doctor of Science (Physics) degree at 2013. Currently, he is the head of the Department of Physics of Semiconductors and Microelectronics at YSU. Since 2015, he is a Full Professor and Senior Researcher at YSU. He is an author of two course-manuals. He has published more than 60 scientific papers in widely reputed journals and has been invited and delivered invited talks in more than 20 International Conferences, as well as author of 3 Patents. H-index: 11. Fields of scientific interests: Physics of semiconductors and semiconductor devices; Semiconductor materials science and technology; Infrared and thermo-photovoltaic devices; Nanoelectronics and nanotechnology. He has been granted four times by the Deutsche Akademische Austauschdienst (DAAD) Awards and performed numerous research visits to Germany. In 2014, he was granted by Chinese Academy of Sciences (CAS) and worked as a Research Professor in CAS Institute of Semiconductors. He is a member of World Renewable Energy Network, member of the Asia-Pacific Chemical, Biological and Environmental Engineering Society, IAAM Gold Medal laureate for 2017 year, as well as he was awarded by YSU Gold Medal at 2020. He is an Editor-in-Chief of "Journal of Contemporary Physics" (Springer) and "Armenian Journal of Physics" (National Academy of Sciences of Armenia).

Abstract: Within the recent decades, much effort has been invested in the growth of quantum dots (QDs), motivated by their unique physical properties. These properties are making them attractive for optoelectronic and other semiconductor devices, single photon sources, quantum computing systems, nanophotonics and quantum optics, as well as for new generation QD-photodetectors and other nanooptoelectronic devices. At the growth of multicomponent composition QDs and QD-molecules (QDMs), a redistribution of components occurs during the strain relaxation. Certainly, over the past several years many scientific and technological investigations were performed to explore graded composition QDs (GCQDs). Previously, several types of nanostructures in InAs-InSb-InP material system were grown, in particular lens-shaped and ellipsoidal QDs, quantum rings, and QDs-nanoleaves cooperative structures as a new type of QDMs.

The nucleation process, characterization and possible applications of GCQDs and QDMs grown from In-As-Sb-P composition liquid phase using Stranski–Krastanow growth mode are presented. AFM investigations show that the massive of QD-structures grown on an InAs (100) surface mainly consists of single conical GCQDs, as well as laterally double, triple, quadruple and quintuple QDMs (Fig. 1). Surface concentration of QDMs was up to two order lower than that of single QDs. QDs growth process was stopped at the initial stage of Ostwald ripening and coalescence to overcome further coarsening. Characterization shows that the QDs average diameter to height ratio equals to ~9, surface density ranges from 5 to 8×109 cm-2 with heights and diameters from 5 nm to 25 nm and 20 nm to 140 nm, respectively. Gauss-like distribution on the dependence of QDs number versus both average diameter and height was observed.

The experimental and quantitative studies of uncapped In (As,Sb,P) double quantum dots (DQDs),suited for

application in novel resonant tunneling nanodiods or single-photon nanooptical up- and downconverters in the mid-infrared spectral range are presented. Details on the growth process using epitaxy from the quaternary liquid phase, as well as the characterization using atomic force microscopy and scanning electron microscopy are presented. We find that most type-II DQDs exhibit an asymmetry such that the two QDs of each pair have different dimensions, giving rise to correspondingly different quantum confinement of hole states (in our material system) localized in each QD. Based on these data, we have performed simulations to identify the relationship between QD dimensions and the energy difference between corresponding confined hole states in the two QDs. Finally, we have determined the strength of an applied electric field required to energetically align the hole ground states of two QDs of different dimensions in order to facilitate hole tunneling. QDs massive optical properties measurements show the enlargement of absorption spectra to long (up to ~3.8 μm) wavelength region at room temperature. Additionally, an idea of DQDs application in new generation opto-electronic devices will be presented.

16:30-16:50 | Paper ID: 8 | Junjun Qi, Xidian University

Speech Title: Knowledge-Guided Neural Network Based Nonlinear Current Model With Combined Loss Function

Author(s): Junjun Qi, Hongliang Lu, Silu Yan, Zhiwu Jiang, Lin Cheng, Yuming Zhang

Abstract: A knowledge-guided Neural network (KGNN)-based nonlinear current model of InP heterojunction bipolar transistor (HBT) is proposed. To improve modeling accuracy and consistency, a combined loss function is constructed and modeling consistency checks are implemented during the training of the neural network to penalize violations of the physical laws. The accuracy of the developed nonlinear current model was verified by comparing the measured and simulated pulse IV results.

16:50-17:10 | Paper ID: 36 | Yutao Chen, Sun Yat-sen University

Speech Title: Physical Insight into Single-Event Upsets of DICE Circuits and Hardening Strategy

Author(s): Yutao Chen, Linlin Cai, Jianwen Lin, Zhengxin Zhang, Wangyong Chen, Yi Sun, Haiming Zhang

Abstract: The single-event upset (SEU) effects, caused by ionizing radiation, poses a significant challenge to the reliability of integrated circuits. In this work, we investigate SEU in dual interlocked storage cell (DICE) circuits for the underlying physical mechanisms and mitigating its impact. SEU in DICE circuits is primarily caused by two factors: data pattern and charge sharing. Data pattern is closely related to the signal transmission of the circuits, while charge sharing arises from the diffusion motion of carriers induced by radiation. A novel circuit hardening strategy based on split active area (SAA) is developed, which aims to reduce the susceptibility to single-event upsets. The effectiveness of the SAA scheme is evaluated through TCAD simulations. The results demonstrate that the proposed SAA optimization effectively decreases the occurrence of SEU in DICE circuits, thereby enhancing the overall reliability against radiation.

17:10-17:30 | Paper ID: 107 | Zhen Dou, Xi'an University of Posts and Telecommunications

Speech Title: Simulation Study of Gate-All-Around TFET Based on Polarization Effect

Author(s): Yunhe Guan, Zhen Dou, Jiachen Lu, Weihan Sun, Haifeng Chen

Abstract: The potential of Tunnel Field-Effect Transistors (TFETs) in overcoming the limitation of the 60 mV/dec subthreshold swing has attracted considerable attention. This paper proposes a gate-all-around TFET based on polarization effects, termed Gate-all-around-Polar-TFET (GAA-P-TFET), to further optimize the performance of TFETs, including reducing the subthreshold swing (SS) and improving the on/off current ratio ION/IOFF. After simulation analysis using Sentaurus TCAD, the SS of GAA-P-TFET can be reduced to as low as 6.7 mV/decade at a drain voltage of 0.5 V, and the highest order of magnitude of the on/off current ratio can reach to 12.

17:30-17:50 | Paper ID: 177 | Chenyang Zhang, Shanghai Jiao Tong University

Speech Title: A New Framework to MOS Device for Cryogenic Application: Linking Materials with Modeling

Author(s): Chenyang Zhang, Maokun Wu, Miaojia Yuan, Yongkang Xue, Pengpeng Ren, Runsheng Wang, Zhigang Ji

Abstract: We proposed a novel framework that links the channel material property with the MOS device physical model for their cryogenic application. Due to subthreshold swing saturation and current inflection phenomenon

at cryogenic temperature, the physical model for the band tail state of cryogenic MOSFET has gained widespread recognition and application, demonstrating a strong correlation with experimental outcomes. Despite the broad acceptance and empirical success of this model, its reliance on a simplified DOS model introduces potential inaccuracies in the extraction of band tail state parameters, and limits its applicability to other channel materials. Here, we propose and implement, for the first time, the calculation of DOS using DFT rather than the simplified 2-dimensional electron gas (2DEG) model. Our results not only align with those derived from simplified models but also extend their application to other alternative channel materials (like SiGe) and provide simulation predictions. This advancement marks a significant leap forward in screening optimal channel materials for use at cryogenic temperatures, potentially revolutionizing the design and performance of MOSFETs in cryogenic applications.

17:50-18:10 | Paper ID: 91 | Binbin Zheng, Southeast University

Speech Title: Simulation of MEMS Microfabrication Process Based on Narrow Band Level Set and Ray Tracing Methods

Author(s): Binbin Zheng, Zaifa Zhou, Jiyang Liu, Suxin Bao, Qingan Huang

Abstract: To improve the efficiency of MEMS device design and development, a MEMS process simulation program has been developed. In this paper, an evolutionary algorithm for surface contours, narrow band level set method, is introduced. The surface rate of the machined material is calculated by the process physics model and the ray tracing method. The surface rate and evolution algorithm are coupled to simulate the morphology evolution of the process. The simulation program is written in C++ language, and the most time-consuming part of the program is accelerated in parallel.

TECHNICAL SESSION

TS19. The Future of Placement

Chair: Jianli Chen, Fudan University

Time	13:30-15:10 | May 13, 2024	Venue	2-6 / Baoji Hall

TAIK DETAILS

13:30-13:50 | Paper ID: 47 | Yuejiao Wang, Fudan University

Speech Title: A Novel Automatic Placement Generation Tool for Current Mirror in Analog Circuits

Author(s): Yuejiao Wang, Lining Wang, Bijian Lan, Jing Wan

Abstract: Analog layout design lacks effective automation tools and is still performed manually. For the placement of current mirror which is one of the most important building blocks in the analog circuit, existing methods typically rely on the common centroid technique, and do not include cascode current mirrors with various transistor lengths. This paper developed an automatic placement generation tool utilizing procedural method, which is applicable to all current mirror variants. This tool generates a diverse set of valuable solutions and automatically performs de-duplication and filtering. The solutions exhibit optimal aspect ratios and area occupancy, with improved routability and reduced wire length during routing.

13:50-14:10 | Paper ID: 70 | Zhiyang Chen, Tsinghua University

Speech Title: Differentiable Rectilinear Steiner Trees for Analytical Placement

Author(s): Zhiyang Chen, Hailong Yao, Tsung-Yi Ho, Ulf Schlichtmann, Xia Yin

Abstract: Placement for very large-scale integrated (VLSI) circuits is a crucial stage for design closure. The wirelength model is a critical ingredient in modern analytical placers, which significantly impacts the overall design quality. Various models have been proposed to smoothly approximate the half-perimeter wirelength (HPWL), such as weighted average. However, during the routing stage, nets are typically routed by rectilinear Steiner trees (RSMT). It has been empirically shown that HPWL cannot accurately approximate the routing wirelength, which induces notable sub-optimality. In this work, we analyze the approximation errors of HPWL model, and theoretically prove the effectiveness of the RSMT-based wirelength model. Moreover, we propose the first differentiable RSMT wirelength model based on the classic RSMT algorithm, which is integrated into the state-of-the-art analytical placer. Experimental results show that our wirelength model improves RSMT wirelength by ~3.5% on average compared with the HPWL-based model on ISPD-2005 placement benchmarks.

14:10-14:30 | Paper ID: 136 | Hong Liu, Southeast University

Speech Title: Effective Legalization with Cell Version Replacement for Hybrid-Row-Height Circuit Designs

Author(s): Hong Liu, Xiqiong Bai, Ziran Zhu

Abstract: In traditional circuit designs, rows within the placement region typically have uniform height. However, a novel hybrid-row-height design paradigm has recently emerged, integrating tall and short rows within the placement region. This innovative approach enhances optimization opportunities for power, performance, and area. Nevertheless, it poses new challenges in placement legalization due to the heterogeneous row and cell structures. Therefore, this paper proposes an effective legalization algorithm with cell version replacement for hybrid-row-height circuit designs. Our approach takes full advantage of multiple versions of the same cell, each with varying dimensions (heights and widths), to incorporate a mechanism for cell version replacement throughout the legalization process. This consideration can help to obtain a legal placement that more closely resembles the global placement, consequently mitigating the increase in half-perimeter wirelength (HPWL). Simultaneously, it can ensure that the tall-row and short-row resources are not overused, avoiding a non-legal placement. Compared with a baseline and a recent work, experimental results show that our algorithm can achieve the smallest HPWL and runtime.

14:30-14:50 | Paper ID: 50 | Zhihui Deng, Shanghai Jiao Tong University

Speech Title: Chiplet Placement Order Exploration Based on Learning to Rank with Graph Representation

Author(s): Zhihui Deng, Yuanyuan Duan, Leilai Shao, Xiaolei Zhu

Abstract: Chiplet-based systems, integrating various silicon dies manufactured at different integrated circuit technology nodes on a carrier interposer, have garnered significant attention in recent years due to their cost-effectiveness and competitive performance. The widespread adoption of reinforcement learning as a sequential placement method has introduced a new challenge in determining the optimal placement order for each chiplet. The order in which chiplets are placed on the interposer influences the spatial resources available for earlier and later placed chiplets, making the placement results highly sensitive to the sequence of chiplet placement. To address these challenges, we propose a learning to rank approach with graph representation, building upon the reinforcement learning framework RLPlanner. This method aims to select the optimal chiplet placement order for each chiplet-based system. Experimental results demonstrate that compared to placement order obtained solely based on the descending order of the chiplet area and the number of interconnect wires between the chiplets, utilizing the placement order obtained from the learning to rank network leads to further improvements in system temperature and inter-chiplet wirelength. Specifically, applying the top-ranked placement order obtained from the learning to rank network results in a 10.05% reduction in total inter-chiplet wirelength and a 1.01% improvement in peak system temperature during the chiplet placement process.

14:50-15:10 | Paper ID: 145 | Haiming Lin, Fuzhou University

Speech Title: Subgraph Matching with Diversity Handling and Its Applications to PCB Placement

Author(s): Chuandong Chen, Haiming Lin, Miaodi Su, Huan He, Jianli Chen, Ziran Zhu

Abstract: Printed circuit board (PCB) placement is a critical stage in industrial chip design, which still heavily relies on manual methods, leading to substantial design time consumption. Given the frequent occurrence of similar or identical modules in different PCB designs, the reuse of placements emerges as a promising avenue to enhance the efficiency of PCB placement. In this paper, we propose a subgraph matching based reference placement algorithm to achieve PCB placement reuse, thereby improving placement efficiency. We first take the netlist of the already placed and unplaced circuits as input and abstract them into graphs. Then, we construct and filter candidate spaces based on the characteristics of components and nets. In the process of filtering candidate spaces, we adopt diversity handling that includes cut edges and block nodes to ensure the proposed algorithm can handle inexact matching. Finally, we introduce virtual nodes to construct a matching tree using a combination of depth-first search (DFS) and breadth-first search (BFS), and then perform hierarchical matching based on this matching tree to complete the subgraph matching and obtain the placement results. Experimental results show that in large-scale PCB cases, our algorithm runs much faster than the state-of-the-art works. Particularly, the matching rate of our algorithm is almost 100% for the tested cases.

TECHNICAL SESSION

TS20. Design Space Exploration

Chair: Yue Wu, Hangzhou Dianzi University

Time	13:30-15:10 | May 13, 2024	Venue	3-6 / Yulin Hall

TAIK DETAILS

13:30-13:50 | Paper ID: 144 | Yuting Cai, Hangzhou Dianzi University

Speech Title: A Logic Optimization Method Using Reinforcement Learning

Author(s): Yuting Cai, Yue Wu, Xiaoyan Yang, Zhufei Chu

Abstract: With the increasing complexity of designs, it is hard to expect certain fixed optimization sequences to generate optimum results for all designs. Automating the space exploration of optimization sequences for a design attracted a good trend of research work using deep learning methods. In this paper, we introduce a framework designed to generate scripts for executing logic synthesis flows. The framework integrates a novel precisely quantified multi-objective reward function and leverages mapped netlist circuit features to enhance state representation within the reinforcement learning paradigm. Experimental results on the EPFL dataset show that the proposed method outperforms existing exploratory methods in terms of area reduction while meeting delay constraints.

13:50-14:10 | Paper ID: 49 | Yang Zhang, Southeast University

Speech Title: An Energy-efficient Multiplier Using Hybrid Approximate Logic Synthesis for Mixed-quantization CNNs

Author(s): Yang Zhang, Qingwen Wei, Hao Cai, Bo Liu

Abstract: Approximate computing is an emerging paradigm that, by relaxing the requirement for full accuracy in convolutional neural networks (CNNs), offers benefits in the design area and power consumption. In circuit design, approximate logic synthesis (ALS) is to discover and synthesize the approximate circuits automatically, given an exact circuit description. This paper proposes a Hybrid ALS Flow which composes Re-partition XOR-BMF ALS and Cartesian Genetic Programming ALS (CGP-based ALS), and designs the Hessian-aware Mixed-quantization CNNs. This paper designs an 8-bit approximate multiplier using the proposed Hybrid ALS Flow and applies it to the Mixed-quantization CNNs. Experiments show that the proposed Re-partition XOR-BMF ALS has better design space exploration than the BLASYS. Compared to the exact Multiplier, the designed approximate multiplier reduces the power delay product (PDP) by 56.17% under an industry 28nm process technology with the power supply of 0.8V, while the accuracy loss is only 1.33% and 2.36% in VGG16 and Resnet50 on CIFAR100.

14:10-14:30 | Paper ID: 73 | Kunlong Li, Fudan University

Speech Title: TLED: Training-Based Approximate Layer Exploration in DNNs with Efficient Multipliers

Author(s): Kunlong Li, Zhen Li, Lingli Wang

Abstract: Deep Neural Networks (DNNs) have demonstrated exceptional capabilities in complex tasks, driving advancements in computation methods, notably through approximate computation. This approach, particularly with approximate multipliers, is crucial for DNN accelerators. Achieving a high-performance accelerator requires not only selecting suitable approximate multipliers but also fine-tuning the network's weights. Traditional methods treat these steps separately. Our innovation introduces trainable TLED-layers, integrating multiplier updates and weight tuning. The method integrates parameterized approximate multipliers into layers, enabling direct hardware optimization in the loss function. This allows for network training using conventional methods after layer replacement. This method optimizes both hardware efficiency and accuracy, as evidenced in MNIST and CIFAR-10 evaluations. Results show a hardware-friendly accelerator on LeNet, reducing the product of power, delay, and area by 10.17% compared to state-of-art approximate multipliers, and a design with only

0.25% accuracy loss yet offering a substantial the product of power, delay, and area decrease of 75.82%. For AlexNet, our approach achieves the highest accuracy among both precise and approximate multipliers. Experimental findings affirm the superiority of our proposed methodology over prior designs.

14:30-14:50 | Paper ID: 4 | Yiqing Mao, Fudan University

Speech Title: PWL-Explorer: A Reconfigurable Architecture for Nonlinear Activation Function with Automatic DSE

Author(s): Yiqing Mao, Huizhen Kuang, Wai-Shing Luk, Lingli Wang

Abstract: Nonlinear functions are indispensable parts of deep neural networks (DNNs). Based on the piecewise approximation with the non-uniform segmentation strategy, this paper proposes PWL-Explorer, a highly parameterized reconfigurable nonlinear core designed with Chisel to implement diverse nonlinear functions. Additionally, we model the design space exploration (DSE) as a multi-objective black-box optimization problem via Bayesian optimization to explore the Pareto front of PWL-Explorer for the precision and area-delay product (ADP) objectives. The experimental results show that compared to state-of-the-art work for element-wise activation functions, the optimized PWL-Explorer architecture achieves an average of 1.58x better ADP while obtaining 2.93x higher maximum absolute error (MAE) precision. Compared to state-of-the-art work for Softmax, PWL-Explorer achieves 1.05x better ADP while obtaining 40.01x better mean square error (MSE) precision. Due to the elaborate hardware design and push-button workflow, PWL-Explorer can provide support to DNN accelerator developers.

14:50-15:10 | Paper ID: 189 | Wangzhen Li, Fudan University

Speech Title: High-Dimensional Analog Circuit Sizing via Bayesian Optimization in the Variational Autoencoder Enhanced Latent Space

Author(s): Wangzhen Li, Zhaori Bi, Xuan Zeng

Abstract: High-dimensional analog circuit sizing with machine learning-based surrogate models suffers from the high sampling cost of evaluating expensive black-box objective functions in huge design spaces. This work addresses the sampling efficiency challenge by elaborately reducing the dimensionality of the input spaces, enabling efficient optimization for automated analog circuit sizing. We propose a latent space optimization method that includes an iteratively updated generative model based on a variational autoencoder to embed the solution manifold of analog circuits to a low-dimensional and continuous space, where the latent variables are optimized using Bayesian optimization. The effectiveness of the proposed method has been verified on two real-world analog circuits with 18 and 59 design variables. In comparison with BO in the original high-d spaces or latent lowd spaces assisted by other embedding strategies, the proposed method achieves 23%˜73% improvements in optimization performance within the same runtime limitations. We also conduct a technology migration experiment using the pre-trained variational autoencoder model, which demonstrates the necessity of pre-training and the scalability of the proposed method.

TECHNICAL SESSION

TS21. Innovative Pathways in Routing

Chair: Gang Chen, Nanjing Industrial Innovation Center of EDA

Time	13:30-15:10 | May 13, 2024	Venue	2-1 / Xianyang Hall

TAIK DETAILS

13:30-13:50 | Paper ID: 149 | Jienan Chen, University of Electronic Science and Technology of China

Speech Title: Routing Generative Pre-Trained Transformers for Printed Circuit Board

Author(s): Hao Wang, Jun Tu, Shenglong Bai, Jie Zheng, Weikang Qian, Jienan Chen

Abstract: In recent years, the growing integration density of electronic devices has presented significant challenges for Printed Circuit Boards (PCBs), with routing emerging as a particularly intricate and labor-intensive task. In this work, we introduce a new routing method, PCB Routing GPT (PRG), leveraging Generative Pre-Trained Transformers (GPT) in the PCB domain. Our approach tokenizes routing patterns, transforming the routing process into token encoding, and facilitating database creation akin to a language model. PRG employs a fusion structure, integrating start and end position information with current flow encoding to predict flow encoding for each wire. In contrast to traditional methods relying on trial and error, PRG's pre-training phase learns from the routing of human experts, summarizing routing patterns effectively. Moreover, PRG resolves wire entanglement issues encountered in traditional routing by employing a parallel routing strategy, enhancing efficiency. Utilizing a Transformer architecture enables GPU acceleration, leading to significant improvements in routing density and speed, achieving state-of-the-art results.

13:50-14:10 | Paper ID: 61 | Weiqing Ji, University of Science and Technology Beijing

Speech Title: LoopRoute: A Fast and Efficient Routing Method for Die-to-Die UCIe Interconnections

Author(s): Weiqing Ji, Haochang Tian, Fei Li, Hailong Yao

Abstract: Recently, chiplet-based designs, also called multi-die systems, have gained significant attention in the semiconductor industry as a promising alternative to extend the Moore's Law in the third dimension. However, the difficulty of interoperability between chips from different vendors has posed a significant challenge for the successful design and operation of multi-die systems. Universal Chiplet Interconnect Express (UCIe) has been proposed to address this issue by standardizing die-to-die connectivity in multi-die systems, which brings new challenges to the die-to-die interconnection problem. This paper presents the first fast and efficient routing method, called LoopRoute, for die-to-die interconnections under the UCIe standard, which significantly accelerates the routing process and enhances routing scalability for large-scale multi-die systems. Compared with the integer linear programming (ILP)-based method, LoopRoute achieves a speedup of more than 200×, while the wirelength increment is less than 0.08%. LoopRoute also shows promise in routing large-scale problems with up to 100k nets efficiently.

14:10-14:30 | Paper ID: 69 | Ze Yang, Fuzhou University

Speech Title: Simultaneous Escape Routing Algorithm for Large-scale Pin Arrays

Author(s): Ze Yang, Kunwei Hu, Qinghai Liu, Jiarui Chen

Abstract: Escape routing is a crucial step in printed circuit board (PCB) design. In response to the issues of low wiring efficiency in large-scale pin array circuit board routing where multiple devices synchronization is not considered in the current escape algorithm, this paper proposes a simultaneous escape routing algorithm based on weighted maximum independent set. Firstly, a path conflict graph is constructed by projecting paths correlated to pin pairs, followed by obtaining layered ordering results using the weighted maximum independent set model. Subsequently, channel estimation and channel optimization are performed using depth-first search in different directions. Finally, an escape routing is conducted using a detailed grid-based wiring method.

Experimental results demonstrate that the proposed algorithm achieves a near 100% successful routing rate for large scale pin array PCB cases. It outperforms the minimum cost multi-commodity flow (MMCF) algorithm and the sequential escape algorithm with estimated functions by an average im provement of 10% in wire length.

14:30-14:50 | Paper ID: 13 | Junkang Jiang, Fuzhou University

Speech Title: Detailed-Routability-Driven Global Routing with Lagrangian-Based Rip-up and Rerouting

Author(s): Junkang Jiang, Pengju Yao, Wenxing Zhu

Abstract: Routing is the most time-consuming phase in the physical design of modern integrated circuits. A carefully designed global routing needs to maximize the routability for the detailed routing while minimizing the wire length and the number of vias. In this paper, we propose a gradient ascent algorithm to solve the 3D global routing ILP model. This algorithm uses the Lagrangian-based cost update method that can more accurately reflect congestion for guiding the global router to generate a solution with fewer vias and congestion. In the gradient ascent rip-up and reroute stage, we use a DAG-based multi-pattern routing strategy to handle highly congested nets with constructed multiple routing patterns. Furthermore, we propose a congestion-aware dynamic net ordering algorithm to improve the congestion convergence of the rip-up and rerouting stage. Experimental results on ICCAD'19 contest benchmarks show that, on average our global router obtains high-quality results, reducing the number of vias by over 1% and 370.6% reduction in DRVs compared to CUGR 2.0, and outperforms TritonRoute-WXL's global routing in terms of runtime consumption and the number of vias.

14:50-15:10 | Paper ID: 141 | Yantao Yu, Fuzhou University

Speech Title: Multi-Strategy Bus Deviation-Driven Layer Assignment Algorithm

Author(s): Yantao Yu, Zepeng Li, Jiarui Chen, Xing Huang, Genggeng Liu, Ning Xu

Abstract: In modern very large-scale integration (VLSI) design, the solution quality of the bus routing is a crucial factor that determines the timing and power of circuit, and finally affects the performance and yield of chips. Taking bus deviation as the main optimization objective, an effective multi-strategy bus deviation driven layer assignment algorithm is proposed to solve the timing-matching problem of bus routing. First, a net priority determination method that integrates multiple features is presented to determine the layer assignment order, thus obtaining a routing sequence which can weigh the wirelength and bus deviation well. Second, an effective single net layer assignment algorithm is proposed to assign each net based on dynamic programming, thus reducing the number of vias. Third, a layer shifting strategy based on the bus lookup table is designed to effectively balance total wirelength and bus deviation by sacrificing a certain number of vias. Experimental results, compared to existing work, show that the proposed algorithm can achieve significant optimization on the bus deviation and total wirelength, and finally obtain the best results in terms of the bus deviation, which is the most important optimization objective for bus routing.

TECHNICAL SESSION

TS22. Exploring EDA Applications in HPC and AI

Chair: Handing Wang, Xidian Univerisity

Time	13:30-15:40 | May 13, 2024	Venue	3-3 / Hanzhong Hall

TAIK DETAILS

13:30-14:00 | Invited Talk | Xinliang Wang, Huawei

Speech Title: Build ARM-based EDA Competitiveness with Software and Hardware Collaborative Optimization

Invited Speaker's Bio: Xinliang Wang, Ph.D., graduated from the Department of Computer Science and Technology, Tsinghua University in 2018. In 2016, as the first student author, he won the Gordon Bell Prize, one of the highest awards in the field of HPC. During his doctoral period, he mainly focused on numerical computing and parallel computing, and he published many papers in top conferences/journals in the field of HPC, including PPOPP, SC, IPDPS, etc. In 2021, he joined Huawei and currently focuses on the research of sparse linear solvers.

Abstract: The rapid development of the EDA industry requires robust computing infrastructure. These foundations support the EDA toolchain and include hardware components such as computation, storage, and networking, as well as software components like compilers, schedulers, mathematical libraries, solvers, operating systems, and development tools. Among these, mathematical libraries and solvers are crucial for enhancing EDA tool performance, while compilers and performance tools play a key role in developing and debugging EDA software. Additionally, schedulers are essential for stable and efficient operation of EDA clusters. In this report, we will focus on the computing infrastructure, using OPC as a typical case, and highlight Huawei's key achievements in software infrastructure.

14:00-14:30 | Invited Talk | Xiaoming Liu, Empyrean Technology

Speech Title: New EDA Ecosystem based on Collaborative Innovation of Software and Hardware

Invited Speaker's Bio: Michael Liu is the senior EDA product director of Empyrean Technology. With more than 10 years EDA products development and management experience, he helps Empyrean built up a mature Analog/Mixed-Signal design flow for power IC market, a unique full customer design EDA solution for flat panel display market,and extended it to Memory, RF, Optoelectronic and other analog related design solutions. He proposed a collaborative reliability design methodology for design and manufacturing, a Yield PPA oriented digital chip design methodology, and further expanded it for different segmented market applications. The solutions are widely adopted by national and international leading design houses.

Abstract: The market demand for integrated circuits is driving the development of EDA technology towards intelligence, systematization, and precision. Industrial driven coupled with technological innovation is the path to the future development of EDA. China has a good environment for industrial and technological innovation. Domestic EDA is in an era of transformation. Traditional EDA technology has placed more emphasis on algorithm innovation, and the computing power and system of hardware have become constraints on the development of EDA. Collaborative innovation combining software and hardware will be the path to future development. This presentation will share the latest applications and progress of Empyrean in Kunpeng ARM computing ecosystem.

14:30-15:00 | Invited Talk | Yutao Ma, Primarius

Speech Title: Building Application-driven EDA Ecosystem Based on ARM-powered Computing Platforms

Invited Speaker's Bio: Dr. Yutao Ma graduated from Tsinghua University in 1996 for bachelor and in 2001 for Ph.D. degrees with honor majoring in Microelectronics. Since then Dr. Ma has been working in EDA industry for over 20 years from Celestry to Cadence then Primairus. His expertise is in semiconductor device modeling, circuit simulation, yield analysis area. Dr. Ma is now in Primarius Technologies as VP of R&D leading technology innovation and new product development as well as the R&D engineering infrastructure team. He also serves as the director of the EDA Innovation Key Laboratory of Shandong Province and the co-director of Primarius-Peking University DTCO innovation laboratory. Dr. Ma published dozens of technical papers in leading journals and conference and held multiple patents in device modeling, simulation algorithm, yield analysis and hardware acceleration.

Abstract: The Electronic Design Automation (EDA) industry faces with ever-increasing complexity in semiconductor design and the need for more efficient, scalable computing solutions. This presentation will explore the transformative potential of ARM-powered computing platforms in enabling a new generation of application-driven EDA ecosystems. By harnessing the energy efficiency, performance, and flexibility of ARM-based systems, Primarius EDA solutions can significantly enhance circuit simulation and verification, physical design and verification, and standard cell library characterization.

We will delve into specific technical applications and academic research outcomes related to the deployment of ARM-powered computing in various facets of the EDA flow, from SPICE simulations that leverage the unique capabilities of ARM processors to the characterization of standard cell libraries optimized for the next generation of chip design. Through case studies and comparative analyses, we will demonstrate how these ARM-based EDA solutions not only meet the current demands of the semiconductor industry but also pave the way for future innovations.

In addition to discussing the technical benefits, this presentation will highlight the importance of collaboration between EDA vendor and IC designers in fostering a vibrant, application-driven EDA ecosystem. With ARM-powered computing platforms at the forefront, we are poised to overcome the limitations of traditional EDA approaches, ushering in a new era of efficiency and innovation in semiconductor design.

15:00-15:20 | Paper ID: 2 | Yangdi Lyu, The Hong Kong University of Science and Technology (Guangzhou)

Speech Title: CAPEDL: Cycle-Accurate Power Estimation with Deep Learning

Author(s): Tong Liu, Haoyu Zhao, Yangdi Lyu

Abstract: A cycle-accurate power estimation model plays a crucial role in the early stages of chip design, which can assist the chips to meet the power, performance, and area (PPA) requirements. PPA are critical factors in determining the overall quality and success of a chip design, as they directly impact its efficiency, speed, and cost-effectiveness. While commercial electronic design automation (EDA) tools such as PrimeTimePX are currently employed for power analysis, their efficiency remains notably low. In this paper, we propose a novel framework, named CAPEDL, which can address the limitations of traditional approaches and improve the accuracy of power consumption estimation. CAPEDL utilizes a two-step deep learning network comprising an auto-encoder network for signal compression and a multilayer perceptron (MLP) model for power estimation. We use various circuits to evaluate the effectiveness of the CAPEDL framework. The experimental results show that CAPEDL outperforms the state-of-the-art approaches, with a normalized root mean squared error (NRMSE) of less than 3% and an average power error of less than 1%.

15:20-15:40 | Paper ID: 38 | Sichao Yang, X-Epic Ltd.

Speech Title: FormalEval: A Method for Automatic Evaluation of Code Generation via Large Language Models

Author(s): Sichao Yang, Ye Yang

Abstract: One of the promising applications of Large Language Models (LLMs) is code generation. However,

evaluating the quality of the generated code poses a significant challenge. Existing evaluation methods such as Rouge or HumanEval have limitations in terms of accuracy or efficiency. In this paper, we propose a formal evaluation tool called FormalEval, which automates the process of checking generated code without the need for manual test case curation. We evaluated our method on common tasks related to Register-Transistor-Level (RTL) Verilog and SystemVerilog Assertions (SVA) generation in the field of Electronic Design Automation (EDA). Our method not only identifies 23% of evaluation error in existing RTL benchmarking dataset, but also fixes the error via test case augmentation. We show FormalEval can help to identify better LLM prompting techniques on SVA generation task. Our method demonstrates state-of-the-art accuracy on the testing dataset.

TECHNICAL SESSION

TS23. Revolutionizing Timing Analysis

Chair: Chen Xi, HEXIN EDA Inc.

Time	13:30-15:10 | May 13, 2024	Venue	2-9 / Presidium Room

TAIK DETAILS

13:30-13:50 | Paper ID: 77 | Longze Wang, Beihang University

Speech Title: Static Timing Analysis Acceleration to Attack Process Corner Explosion by Matrix Filling Prediction

Author(s): Longze Wang, Zhelong Wang, Wei X. Xing, Ning Xu, Yuanqing Cheng

Abstract: Static timing analysis (STA) is a highly effective procedure required for modern advanced nanoscale integrated circuit design. However,the increasing number of process corners has made performing STA analysis at each physical design stage time-consuming. To enhance efficiency, we propose MCSTA, a point-wise imputation method, to predict timing path delay under different process corners. We formulate it as a partial matrix completion problem and solve it using a neural network-based timing prediction algorithm. Unlike previous methods that rely on full-timing simulations under the specific process corner, our algorithm captures timing information from only a few timing paths, significantly reducing run time overhead. We further optimize timing prediction accuracy using autoencoders to capture relationships between timing paths and process corners. Additionally, we introduce an active learning algorithm adapted for point-wise imputation to utilize timing information from previous design stages, minimizing the required number of timing simulations and improving prediction performance. Experimental results show that our method achieves nearly 100% accuracy with a limited number of path timings while reducing run time overhead by orders of magnitude compared to conventional STA analysis.

13:50-14:10 | Paper ID: 113 | Shuhao Jia, Southeast University

Speech Title: Aging-aware Path Timing Prediction via Graph Representation Learning

Author(s): Shuhao Jia, Chuanfang Jiang, Huan Liang, Jitao Yu, Aiguo Bu

Abstract: In advanced CMOS technology, aging degradation dominated by Negative Bias Temperature Instability (NBTI) has emerged as a significant challenge for the timing closure of circuits. Accurate aging-aware static timing analysis (STA) at the early design phase is critical for establishing appropriate timing margins to ensure circuit reliability throughout the chip lifecycle. Traditional aging-aware timing analysis flows find it difficult to achieve a tradeoff between computational overhead and accuracy. In this paper, we propose an aging-aware path timing prediction framework via graph representation learning. We customize a graph transformer network (GTN) to generate efficient path graph representation with global attention mechanism. Experimental results demonstrate that our proposed framework can obtain accurate timing path prediction with MAPE score of 3.75%, and can achieve acceleration of over 7000 times compared to SPICE simulation with acceptable accuracy loss.

14:10-14:30 | Paper ID: 134 | Ziyin Cui, Southeast University

Speech Title: An Efficient Statistical Clock Skew Analysis Method for Clock Trees

Author(s): Ziyin Cui, Tao Zhang, Yihui Cai, Peng Cao, Ting-Jung Lin, Lei He

Abstract: Increasing process variability poses great challenge in 2D/3D high-performance clock network design. The variation of deivce, interconnect and TSV lead to the clock skew variation. However, in most prior models, the variation was not considered comprehensively, where the effect of the equivalent capacitance variation of the interconnect/TSV on the delay of the device was ignored, leading to poor accuracy for clock tree delay variation. In this work, an efficient statistical clock skew analysis method for clock trees is proposed, which considers the variations of device, interconnect, and TSV in 2D/3D clock trees together, and considers the cap variation impact on device variation during the bottom up propagation algorithm. The proposed model was

validated under TSMC 22nm process by 3D clock trees implemented for artifical H-tree structed cases and ISCAS'89 benchmarks. Our model demonstrates excellent agreement with golden Monte Carlo simulation results in terms of the standard deviation of maximum clock skew with the average error of 2.35% while achieves 1400 times speed up. Comparing with competitive works, our model achieves 1.7 times accuracy improvement with comparative simulation effort.

14:30-14:50 | Paper ID: 158 | Yang Zhang, Xidian University

Speech Title: An Efficient Aged Timing Analysis Method for Digital Integrated Circuit under NBTI Effect

Author(s): Yang Zhang, Zhengguang Tang, Yawei Jin, Hong Zhang, Yongsheng Sun, Chen Chen, Xiaoling Lin, Cong Li, Hailong You

Abstract: With the continuous development of semiconductor technology, the performance and integration of integrated circuits (ICs) have been continuously improved. However, below the 65nm technology node, one of the aged effects of chips, Negative Bias Temperature Instability (NBTI) effect, has become an important factor affecting the performance and reliability of digital integrated circuits. This paper proposes an efficient aged timing analysis method for digital integrated circuit under NBTI effect. The method characterizes standard-cell aged library under a small number of typical input signal probabilities. Based on the established standard-cell aged library, timing model for perceiving NBTI aged is constructed through machine learning regression. The timing model established in this paper includes the mapping relationship between aged-related parameters and corresponding aged timing, with the input signal probability, input signal transition time, and output load capacitance of the cell as inputs, and the delay or output transition time of the cell as output. Based on the established timing model for perceiving NBTI aged, timing simulation of each cell in digital integrated circuits can be performed after degradation. Experimental results indicate that compared to existing methods, the approach presented in this paper reduces aged library usage by approximately 70% while only introducing small timing simulation error.

14:50-15:10 | Paper ID: 195 | Fuxing Deng, China University of Petroleum

Speech Title: SD-SSTA: Statistical Static Time Analysis Algorithm Considering Skewed Distribution

Author(s): Fuxing Deng, Yihang Feng, Dan Niu, Xiao Wu, Zhou Jin

Abstract: Static Timing Analysis (STA) is one of the most widely used and successful analysis engines in digital circuit design in recent years. However, the Deterministic Static Timing Analysis (DSTA) does not take into account the effect of process parameter variability on circuit performance, which arouses people's attention to the ability of STA to effectively simulate statistical changes. Therefore, Statistical Static Timing Analysis (SSTA) has been proposed and extensively studied. Traditional SSTA algorithms, such as probabilistic propagation based on Gaussian distribution and Monte Carlo simulation, cannot achieve a high accuracy and good performance. In this paper, a SSTA algorithm considering skew distribution, SD-SSTA, is proposed, which successfully realizes accurate calculation of;arrival time and timing margin, and has excellent performance. The paper makes three contributions. (1) We convert the non-Gaussian distribution into a Gaussian Mixture Model (GMM), which fits the real result better than the traditional SSTA algorithms. (2) We consider the influence of skew and introduce Skew Adjustment Factor (SAF) into the calculation of timing margin to ensure that the results are more realistic. (3) We use the name mapping method to reduce the memory consumption of the algorithm, which further improves the algorithm memory performance. Compared with SSTA algorithm based on Gaussian distribution, SD-SSTA algorithm has excellent performance in both accuracy and performance.

TECHNICAL SESSION

TS24. Thermal Management at Chip Level

Chair: Min Tang, Shanghai Jiao Tong University

Time	13:30-15:10 | May 13, 2024	Venue	2-5 / Weinan Hall

TAIK DETAILS

13:30-13:50 | Paper ID: 1 | Zhizhu Cao, Hisilicon, Huawei

Speech Title: Study on Compact Thermal Model for 3D Interlayer Electronic Cooling based on Fluid-Solid Coupling Heat Transfer

Author(s): Zhizhu Cao

Abstract: This paper presents a 3D Interlayer Cooling Emulator written in C++ and python language, in which a common Compact Transient Thermal Modeling (CTTM) of solids and fluids based on an equivalent circuit of convection thermal resistances is proposed. Compared to the state of art tools such as 3D-ICE, our previous in-house 3DDCTM fast thermal simulation tool, the present method has the ability of calculating the heat transfer between solid and fluid much more accurately by solving the unsteady heat convection-diffusion problem in the whole domain, rather than using a semi-empirical correlation. To verify the correctness of the proposed method, three typical tests including 3D interlayer cooling are implemented and maximum relative deviation of the junction temperature is 2.83% compared with results from commercial tools demonstrating the high precision of the present tool. Moreover, the proposed Emulator could greatly reduce the calculation time and in the test about 157 times faster than commercial tools are observed.

13:50-14:10 | Paper ID: 89 | Ao Wang, Shanghai University

Speech Title: Rectangular Approximation for Curved-Shape Power Density in Chip Thermal Analysis

Author(s): Ao Wang, Luqiao Yin, Wenxing Zhu, Aiying Guo, Jingjing Liu, Min Tang, Liang Chen, Jianhua Zhang

Abstract: This paper proposes a rectangular approximation method for curved-shape power density to rapidly calculate the temperature profile of the entire chip by using the 2D thermal model with the effective thermal characteristic length. The proposed method employs rectangular blocks to approximate the non-rectangular power density areas, thereby enabling the utilization of stepwise integration for the determination of the cosine series coefficients. In contrast to the conventional grid mesh approach, this rectangular approximation significantly reduces the number of required mesh elements, thus considerably enhancing computational efficiency. Numerical results reveal that the proposed method achieves a speed improvement ranging from 94× to 195× over the traditional grid technique, while maintaining comparable accuracy. Furthermore, the maximum absolute error observed in temperature predictions is limited to a mere 0.37K.

14:10-14:30 | Paper ID: 198 | Kexin Zhu, Tongji University

Speech Title: Hybrid Model-Based Thermal Analysis Methodology for Integrated Circuits

Author(s): Kexin Zhu, Runjie Zhang, Qing He

Abstract: Modern high performance computing chips, such as SoC and CPU, are requiring higher hash rate, which accelerates the integration level of integrated circuits. As the Dennard's law no longer holds, the power density of integrated circuits also increases with the level of integration, which results in the fact that the thermal issue is becoming one of the most important issues limiting the development of integrated circuits. To tackle this problem, a fast thermal analysis methodology for integrated circuits is needed. In this paper, we presents a fast on-chip thermal analysis methodology using a hybrid thermal model. The hybrid thermal model is the combination of the detailed on-chip model and the compact model for the package. We propose a novel thermal analysis flow that separates the construction and reduction of the package from the on-chip thermal simulation. Once the compact thermal model of the package has been extracted, we can combine it with any detailed model

of the chip to perform fast thermal simulation. The experimental results show that our hybrid model achieves a 28X speedup without any accuracy loss.

14:30-14:50 | Paper ID: 64 | Qipan Wang, Peking University

Speech Title: ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D-IC Systems Considering Nonlinear Leakage and Conductivity

Author(s): Qipan Wang, Tianxiang Zhu, Yibo Lin, Runsheng Wang, Ru Huang

Abstract: Thermal simulation plays a fundamental role in the thermal design of integrated circuits, especially 3D ICs. Current simulators require significant runtime for high-resolution simulation, and dismiss the complex nonlinear thermal effects, such as nonlinear thermal conductivity and leakage power. To address these issues, we propose ATSim3D, a thermal simulator for simulating the steady-state temperature profile of nonlinear and heterogeneous 3D IC systems. We utilize the global-local approach, combining a compact thermal model at the global level, and a finite volume method at the local level. We tackle the nonlinear effects with Kirchhoff transformation and iteration. ATSim3D enables local-level parallelization that helps achieve an average speedup of 40× compared to COMSOL, with a relative error <3% and a state-of-the-art resolution of 4096 × 4096, holding promise for enhancing thermal-aware design in 3D ICs.

14:50-15:10 | Paper ID: 72 | Shunxiang Lan, Shanghai Jiao Tong University

Speech Title: Domain Decomposition and Reduction Method for Efficient Thermal Simulation and Design of 2.5D Heterogeneous Integration

Author(s): Shunxiang Lan, Min Tang, Junfa Mao

Abstract: In this paper, an efficient domain decomposition and reduction (DDR) method is proposed for thermal simulation and design of 2.5D heterogeneous integration. Firstly, the DDR method decomposes the integrated system into the core area and the non-core area. Then, the thermal impact of non-core area is represented by the equivalent coupling matrix built up on the interface of two areas, which contributes to confining the solution domain from the whole system to the core area. By this means, the DDR method achieves significant speed-up in the computational efficiency. The accuracy and efficiency of the proposed method is validated through the numerical example, where a 10x speed-up is achieved comparing with the commercial software.

TECHNICAL SESSION

TS25. Device Simulation and Optimization

Chair: Cong Li, Xidian University

Time	16:00-18:00 | May 13, 2024	Venue	2-6 / Baoji Hall

TAIK DETAILS

16:00-16:20 | Paper ID: 202 | Hengyi Liu, Peking University

Speech Title: A Neural Network-based Framework for Accelerated Device-Circuit Electrothermal Co-Simulations in GAAFETs

Author(s): Hengyi Liu, Sihao Chen, Wu Dai, Yu Li, Baokang Peng, Lining Zhang, Runsheng Wang, Ru Huang

Abstract: In this work, an efficient electro-thermal coupling model is developed and validated for 3nm Gate-all-around field effect transistors (GAAFET), which combines the artificial neural network (ANN) model for characterizing electrical properties of devices and a multi-stage RC thermal model with geometry dependence. The temperature rise induced by the self-heating effect (SHE) of the device is evaluated by the RC thermal model and feedback into the ANN model for self-consistent electrothermal interactions, and the number of hidden layers and neural nodes in the ANN model has a significant influence on the simulation accuracy and efficiency. A remarkable acceleration with an acceptable accuracy of electrothermal co-simulation compared with that of the BSIM-CMG circuit simulation framework can be observed, which provides a desirable scheme for thermal-aware reliability assessment at the device-circuit level.

16:20-16:40 | Paper ID: 23 | Wei Du, Nanjing University of Posts and Telecommunications

Speech Title: Automatic Design of Structural Parameters for GaN HEMT Using Genetic Algorithm and Artificial Neural Networks

Author(s): Wei Du, Jing Chen, Jiaohao Wu, Qing Yao, Yufeng Guo

Abstract: In this paper, an automatic optimization technique of structural parameters for gallium nitride high-electron-mobility transistors (GaN HEMT) is proposed. Given the design targets, including breakdown voltage (BV) and specific on-resistance (Ron,sp), this technique can provide the structural parameters of GaN HEMT to meet the targets based on automatic iteration and optimize process using artificial neural networks (ANN) and genetic algorithms (GA). The results show that, when evaluated through technology computer-aided design (TCAD) simulations, designs obtained from the proposed technique deviate from the expected specifications by 2.6% and 0.98%, respectively. Additionally, the efficiency of the proposed method is reflected in its runtime, with the automated design time for each case is within 2 minutes. We believe that the design approach is crucial in accelerating the design closure for GaN transistors.

16:40-17:00 | Paper ID: 93 | Yue-Yang Liu, Institute of Semiconductors, Chinese Academy of Sciences

Speech Title: Atomic Level to Device Level Simulation of Transistor's Reliability

Author(s): Yue-Yang Liu

Abstract: Reliability simulation and design is becoming more and more important with the shrinking of device size and advancing of device architecture. However, the traditional simulation tools are not catching up with the increasing demanding on accuracy and universality, due to the strong reliance on empirical/fitted parameters and oversimplified/phenomenological models. It is highly anticipated to improve the traditional tools by integrating with atomistic simulations and by developing more accurate physical models for various reliability issues; At atomic level, we can not only calculate the parameters for materials and interfaces accurately, but also reveal the microscopic processes or physical mechanisms vividly. Take the bias temperature instability (BTI) issue for example, whose physical origin is defect induced charge trapping and emission, we can conduct first-

principles calculations on realistic semiconductor-dielectric interface models (e.g. Si/SiO2/HfO2), and calculate the key quantities including band alignments, defect energy levels, charge induced reorganization energies, and coupling strength between electronic states. Combing these parameters with charge transfer theories such as Marcus theory and NMP theory, we can obtain the exact charge trapping/emission rates of various defects in a transistor. These rates can be finally put into compact models to generate the macroscopic appearance of reliability issues, e.g. the threshold voltage shift.;;For the hot carrier degradation (HCD) issue, whose physical origin is carrier injection induced defect generation, atomic level simulation can explicitly show which kind of local structure is more likely to be damaged by carriers, how large the energy barrier for defect generation is, how often the carriers of various energies can interact with the defect precursor, and what is the final path of defect generation. The time-dependent density functional theory (TDDFT) allows us to observe the whole process of defect generation directly at real-time. Moreover, the parameters extracted from atomic simulation can be combined with TCAD simulation and physical models to explain the experimental data, and it has been demonstrated by us and collaborators that the hot carrier degradation experimental data can be well modeled to cover a broad range of technologies.

17:00-17:20 | Paper ID: 101 | Hongwei Zhou, Beihang University

Speech Title: Heat Generation Counted by Phonon Absorption and Emission in GAA FET under the Framework of Non-Equilibrium Green's Function Method

Author(s): Hongwei Zhou, Zifeng Wang, Suteng Zhao, Deming Zhang, Lang Zeng

Abstract: As the most promising device beyond FinFET technology, the Gate-All-Around (GAA) field effect transistor (FET) shows excellent electrical characteristics, but also suffers severe self-heating effects, which compromise the performance and reliability of the device. The commonly used Joule heat model fails to investigate the thermal properties of nanoscale devices, and a rigorous treatment of heat generation by counting phonon absorption and emission is demanded. In this paper, we build such a heat generation model for Si GAA nanowire FETs based on the Non-equilibrium Green's function (NEGF) method with the accurate electron-phonon interaction. Both the acoustic phonon scattering and the optical phonon scattering are considered under the self-consistent Born approximation. Since the simple geometry of GAA FETs, an uncoupled mode space approach is adequate and utilized, which alleviates the computation burden dramatically. The Fourier heat equation which takes proposed heat generation model as the heat source is employed in the simulation. The simulation result shows the role of phonon scattering when compared with ballistic transport. The heat source we obtained exhibits similar characteristics to that of the Joule heat model but with a much smaller magnitude. It is also observed that as the channel length decreases, the ratio of heat dissipated in the device decreases, which means that the validity of the Joule heat model becomes even weaker.

17:20-17:40 | Paper ID: 155 | Zhaohai Di, Institute of Microelectronics of the Chinese Academy of Sciences

Speech Title: Virtual Fab Coupled Physics-based Simulation Design of sub-2nm node 3D Heterogeneous 6T SRAM, with Vertical Si GAA CFET and CAA IGZO Pass Gates

Author(s): Zhaohai Di, Yue Zhao, Yanna Luo, Haoqing Xu, Lingfei Wang, Jianhui Bu, Yongliang Li, Zhenhua Wu

Abstract: In this work, we propose an all-vertical-transistor based 3D heterogeneous 6T SRAM design. Self-align Si vertical gate all-around (vGAA) FEOL CFET inverters and vertical channel all around (vCAA) BEOL-compatible IGZO pass gates (PG) are stacked vertically again in 3 layers within a 2T footprint area. State-of-the-art Virtual Fab process emulation validates the hetero-integration flow and generate near realistic geometry of not only the transistor but also the interconnect of a 6T SRAM cell. Furthermore, by physics based simulation augmented fine tuning and extending the experimental validated device compact model and the interconnect RC, geometry- and parasitic-aware device to circuit DTCO analysis of the 3D heterogeneous 6T SRAM is performed. The hetero-integration of IGZO vCAA PG and vGAA CFET inverters showed 59% Read Static Noise Margin (RSNM) enhancement, 86% static leakage power reduction, and 53% area reduction.

17:40-18:00 | Paper ID: 166 | Yuanzhao Hu, Peking University

Speech Title: Optimization of Breakdown Characteristic for SiC MOSFETs by Self-developed Simulator

Author(s): Yuanzhao Hu, Fei Liu, Xiaoyan Liu

Abstract: We have developed a simulator based on semi-classical transport models, which include mobility, generation, and recombination models, to study and optimize the performance and breakdown characteristics of 4H-silicon carbide (4H-SiC) MOSFETs. This simulator matches well with both experimental and commercial TCAD results, proving to be a stable and reliable tool.With this simulator, we studied the dependence of the breakdown voltage on the temperature and the structural parameters of the device, and provided an optimization for enhancing the breakdown voltage. Our findings reveal that adjusting the device structure influences the breakdown voltage more than regulating the temperature.

TECHNICAL SESSION

TS26. Need More Acceleration? Use FPGA!

Chair: Yibo Lin, Peking University

Time	16:00-18:10 | May 13, 2024	Venue	2-5 / Weinan Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Yaowei Zhang, Beijing Microelectronics Technology Institute

Speech Title: HT-TMR: An Efficient Netlist-Level TMR Tool for FPGA SEU Mitigation

Author(s): Yaowei Zhang, Lei Chen, Shuo Wang, Jing Zhou, Chunsheng Tian, Yu Li, Yuanhang Bu, Yuxin Yu

Invited Speaker's Bio: Yaowei Zhang, Master, mainly focused on FPGA radiation mitigation and FPGA EDA software.

Abstract: This paper describes an efficient software tool HT-TMR tool, one of BMTI HongTu series software, developed to automatically apply TMR mitigation on FPGA design to protect against SEUs. The tool provides three preset TMR modes and a custom TMR mode for designers. Once the TMR mode is selected, the tool parses the input EDIF file, determines necessary points to insert the voters, and generates the newly constructed circuit in EDIF format which has the same functionality of the original. Compared with Mentor's Precision Hi-Rel tool, our tool has a lower resource utilization, better timing performance, and higher compatibility.

16:30-16:50 | Paper ID: 133 | Shaoqiang Lu, Shanghai Jiao Tong University

Speech Title: An FPGA-based Multi-Core Overlay Processor for Transformer-based Models

Author(s): Shaoqiang Lu, Tiandong Zhao, Rumin Zhang, Ting-Jung Lin, Chen Wu, Lei He

Abstract: Transformer-based models have achieved extensive success with increasingly large numbers of parameters and computations, for which many multi-core accelerators have been developed. Nevertheless, they suffer from limited throughput due to either low operating frequency or high communication overhead between cores. This paper proposes an FPGA-based multi-core overlay processor, MCore-OPU, to optimize intra-core computation and inter-core communication. First, we boost the operating frequency of the processing element (PE) array to double the rest of the processor to improve the intra-core throughput. Second, we develop on-chip synchronization routers to reduce expensive off-chip memory traffic, where only the partial sum and maximum are communicated between cores rather than entire vectors for layer normalization and softmax. Meanwhile, we optimize the multi-core model allocation and scheduling to minimize the inter-core communications and maximize the intracore computation efficiency. The MCore-OPU is implemented with four cores and four DDRs on the Xilinx U200 FPGA, where the PE array runs 600MHz, and the rest runs 300MHz. Experimental results show that the MCore-OPU outperforms other FPGA-based accelerators by 1.24×–1.39× and A100 GPU by 5.31×–5.81× in throughput per DSP for BERT, ViT, GPT-2 and LLaMA inference, respectively.

16:50-17:10 | Paper ID: 59 | Yiran Zhang, Southern University of Science and Technology

Speech Title: Toward Efficient Co-Design of CNN Quantization and HW Architecture on FPGA Hybrid-Accelerator

Author(s): Yiran Zhang, Guiying Li, Bo Yuan

Abstract: Field programmable gate array (FPGA) has emerged as a promising platform for accelerating convolutional neural networks (CNNs). In this paper, we propose a low-latency CNN hybrid-accelerator system and an efficient design space exploration (DSE) method. Specifically, our targeted FPGA platform consists of different types of accelerators for two advantages: high concurrency and full hardware utilization (i.e., look-up tables (LUTs) and digital signal processors (DSPs)). Besides, we adopt a bandwidth-aware analytical model for

system latency to consider pipeline stalls and computation cycles simultaneously. Furthermore, for the huge design space encompassing layer-wise CNN quantization and FPGA hybrid-accelerator architecture, we propose a DSE method (named DiMEGA) aimed at enhancing search efficiency, which is a differentiable method embedded by a genetic algorithm. The performance of our CNN hybrid-accelerator system is demonstrated on a PYNQ-Z2 FPGA platform. The experimental results show that the system latency can be reduced by 42% ~ 48% without sacrificing accuracy, and the DSE time of DiMEGA is reduced by 23% on ResNet20-CIFAR10, and 63% on ResNet56-CIFAR10, compared with SOTA.

17:10-17:30 | Paper ID: 190 | Shoulin Zhang, Zhengzhou University

Speech Title: DUET: FPGA-Accelerated Differential Testing Framework for Efficient Processor Verification

Author(s): Shoulin Zhang, Ziqing Zhang, Yungang Bao, Kan Shi

Abstract: With the increasing complexity of modern processors, verification becomes the main bottleneck in the entire processor development cycle, which can occupy up to 70% of the development time. Primarily this is because multiple iterations of debugging and software simulations are extremely time-consuming. To improve the verification and debugging efficiency, recent studies investigated differential testing techniques such as DiffTest, which dynamically compares the runtime results from the hardware design-under-test (DUT) and its software reference model. However, the slow speed of software simulation constrains the efficiency and effectiveness of these verification techniques. Although FPGAs can speed up the simulation, current methods either offer limited visibility into design details or are costly when dynamically checking against a reference model at the system level; In this paper, we present DUET, an FPGA accelerated differential testing technique that combines the fine-grained debugging capability of DiffTest and the high simulation speed of FPGA prototyping. We evaluate the proposed method with practical RISC-V processors and demonstrate that the proposed approach accelerates verification efficiency up to 20x while preserving full visibility and debugging capabilities.

17:30-17:50 | Paper ID: 173 | Siyuan Miao, University of California, Los Angeles

Speech Title: An FPGA-based Efficient Streaming Vector Processing Engine for Transformer-based Models

Author(s): Zicheng He, Tiandong Zhao, Siyuan Miao, Chen Wu, Lei He

Abstract: Transformer-based models have obtained extensive success. As their linear operations have been significantly accelerated by a wide range of approaches, nonlinear operations tend to have limited hardware efficiency and become the performance bottleneck. Prior works to accelerate nonlinear operations suffer from either low area efficiency with poor instruction set architecture (ISA) or limited throughput due to the loop-carried dependency in reduce operations. In this paper, we propose a vector processing engine (VPE) with new streaming ISA to achieve flexible streaming execution for nonlinear operations and obtain better hardware efficiency. Moreover, we relax the loop-carried dependency in reduce operations with look-ahead dataflow optimization and improve the throughput of nonlinear operations. Experiment results on Xilinx U200 FPGA show that VPE can outperform other FPGA vector processing units on throughput by 1.14x-3x for softmax, layer normalization, GELU across different vector sizes.

17:50-18:10 | Paper ID: 191 | Zijian Jiang, Beijing University of Technology

Speech Title: Efficient Verification Framework for RISC-V Instruction Extensions with FPGA Acceleration

Author(s): Zijian Jiang, Keran Zheng, Yungang Bao, Kan Shi

Abstract: The RISC-V instruction set architecture (ISA) enjoys the flexibility for domain-specific custom instruction extensions. While the basic RISC-V ISA contains common instructions, the extended accelerators provide additional computing power to meet diverse needs, making it well-suited for various emerging fields. High-level synthesis (HLS) provides a way to build hardware accelerators directly using RTL. It allows software engineers to create complex digital circuit designs using high-level languages such as C/C++, further improving development efficiency. However, verifying a design that includes RISC-V cores and custom extensions can be challenging. Traditional approaches for verifying HLS-generated designs use C-RTL co-simulation, which primarily focuses on the unit level, while making impractical assumptions about interactions between HLS-

generated IPs and the processor. On the other hand, designs that combine RISC-V cores with custom extensions require system-level verification, which must extensively exercise both components and their interconnections. Furthermore, traditional C-RTL co-simulation performs cycle-accurate software simulation, which can be extremely time-consuming. To efficiently verify a RISC-V processor design with custom instruction extensions, we propose a novel verification framework that combines the benefits of the high-level abstraction of C/C++ simulation and cycle-accurate modeling of C-RTL co-simulations. We map the RISC-V core and the HLS-generated custom instruction accelerators, along with their corresponding C/C++ software models, onto the same FPGA with hardened processors allowing them to run simultaneously. A global monitor and checker carefully check the results of both the hardware and software in real-time. If a mismatch is detected, we capture a snapshot of the entire hardware, and reconstruct the simulation in external software simulators for detailed debugging. Through a series of benchmark experiments, results show a significant performance improvement over conventional approaches from 1419x to 9011x.

TECHNICAL SESSION

TS27. Analog Insights: New Waves on Simulation and Analysis

Chair: Guoyong Shi, Shanghai Jiao Tong University

Time	16:00-18:10 | May 13, 2024	Venue	2-1 / Xianyang Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Nan Zhang, Semisight

Speech Title: An Efficient and Versatile Mixed Signal Simulator – MSIM

Invited Speaker's Bio: Nan (Jason) Zhang, Master of Science in Computer Architecture, Department of Computer Science, Institute of Computing Technology. He got his bachelor's degree in Peking University, EE department.

He worked at Cadence since 2007 for more than 15 years. During that time, he focused on Mixed-Signal simulation and verification technology and obtained several US patents.

In 2020, he founded EDA start-up company Semisight, focusing on digital circuit simulation and mixed-signal circuit simulation platform. In 2021, Semisight launched the first domestic EDA tool for automotive functional safety simulation and verification, named SSIM. In 2023, Semisight launched the XSIM production for digital circuit's logic verification. In 2024, Semisight will announce the first domestic mixed-signal simulation tool in unique solution to handle digital and analog design files together with automatic D2A and A2A insertion, named MSIM.

Abstract: In this talk, we briefly introduce a mixed signal simulator from our company, MSIM. The interface between the analog and digital domains is where the complexity arises. Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) play a pivotal role at this interface, translating between the continuous nature of analog signals and the discrete steps of digital signals. MSIM provides the interface elements (IEs), which encapsulate the A2D and D2A components, facilitating the labor needed for the user to design the system. MSIM elaborately handles various difficulties in mixed signal simulation, especially in the interaction between analog and digital counterparts. It not only models these conversion processes accurately but also handles the timing and synchronization of the signals across both domains.

16:30-16:50 | Paper ID: 32 | Yuefan Wang, Xiamen University

Speech Title: Automated Generation Procedure for Fully Differential Op-amp Using TED

Author(s): Yuefan Wang, Qingsen Wu, Yuan Wang, Qian Qin, Jinglei Hao, Chenkai Chai, Yukai Lu, Lin Li, Zuochang Ye

Abstract: This paper proposes an automated generation method which encompasses the entire process from performance specifications to layout for the fully differential gain-boosted operational amplifier (op-amp). At the schematic level, this process uses the gm/ID methodology to automatically explore solution spaces and determine dimension(W/L) of transistors to meet performance constraints. By transition of pre-computed lookup table across technologies, it achieves design migration. At the layout level, leveraging Tsinghua Electronic Design (TED) enables direct conversion of parameter of circuit into layouts. Experimental results show this process can generate sized circuits and layouts meeting requirements across various technology and performance specification.

16:50-17:10 | Paper ID: 48 | Yuan Zhao, Tsinghua University

Speech Title: Design and Implementation of the MTP Compiler

Author(s): Yuan Zhao, Yunlong He, Jianhao Xiao, Zhongbo He, Zuochang Ye, Yan Wang

Abstract: In the semiconductor storage domain, the swift advancement of Static Random-Access Memory (SRAM) has been significantly accelerated by the extensive adoption of so phisticated SRAM Compiler tools.

These instruments enable the rapid generation of tailor-made SRAM memory arrays, effectively addressing specific design requirements. Nonetheless, the development of comparable compiler technologies for other types of memory, such as Multiple-Time Programmable (MTP) memory, has been notably absent. Our study fills this void by introducing a groundbreaking MTP Compiler that is both parameter-driven and compatible across different processes. Leveraging the capabilities of the TED electronic design au tomation tool, this innovative compiler facilitates the expedited production of MTP circuits and layouts for a broad spectrum of capacities, catering to diverse design needs. Its adaptable architecture is especially proficient at accommodating changes in process nodes, significantly reducing the time and effort required for the development of MTP memory technologies. This advancement streamlining the path from concept to production for MTP memories.

17:10-17:30 | Paper ID: 84 | Xisheng Zhang, Shanghai Jiao Tong University

Speech Title: A Subcircuit Matching Approach to Structural Analog Circuit Model Generation and Sizing

Author(s): Xisheng Zhang, Mingzhen Li, Qixu Xie, Guoyong Shi

Abstract: In this paper we study an application of Ohlrich's SubGemini algorithm, a subcircuit matching algorithm, to structural modeling and sizing of CMOS analog integrated circuits with emphasis on multiple-stage circuits including Op Amps and low-dropout (LDO) regulators. Structural modeling can help the design of multiple-stage circuits by introducing structural reduction, structural constraint, and structural mapping, enabling design automation in this field with a traceable circuit manipulation track. Given the fact that a large number of CMOS transistor-level components (cells) are frequently used in analog integrated circuit, we propose to create a library for such commonly used cells and develop a hierarchical subcircuit matching engine (by an adaptation of the SubGemini algorithm) to decompose structurally an analog circuit into a cell form assembly. This work can also be considered a structural circuit recognition work, which can be applied to fast macromodel generation and sizing constraint generation. Procedural details are presented and applications are demonstrated.

17:30-17:50 | Paper ID: 157 | Yiyang Zhao, Fudan University

Speech Title: HD-MCTS: An Analog Circuit Optimization Algorithm Based on High-dimensional Monte Carlo Tree Search

Author(s): Yiyang Zhao, Lemeng Li, Ruiyu Lyu, Zhaori Bi, Changhao Yan, Xuan Zeng

Abstract: With the development of semiconductor technology, the process nodes are being continually reduced. While digital circuit design has been automated throughout the process, the design of analog circuits still relies on manual design. Hence, there is an urgent need to develop automated design tools for analog circuits to improve productivity. In this paper, we propose a method that combines the advantages of Bayesian optimization and dynamic Monte Carlo tree search to obtain the feasible solution space through adaptive clustering, thereby narrowing the search range of the Bayesian optimization algorithm and improving optimization efficiency. For the Ackley test function, low-noise transconductance amplifier and bandgap voltage reference experiments: in comparison with the Trust Region Bayesian Optimization (TuRBO) that is currently available, the optimization outcomes are enhanced by 20.4% to 46.5%, leading to a speedup of 0.95 to 2.62 times. Additionally, in comparison with the LA-MCTS algorithm, the optimization outcomes are improved by 20.4% to 46.5%, resulting in a speedup of 0.96 to 6.55 times.

17:50-18:10 | Paper ID: 210 | Xinyu Yu, Fudan University

Speech Title: Hierarchical Optimization Based on Partial Performance Tradeoff Modeling Method for Large Scale Analog Circuits

Author(s): Xinyu Yu

Abstract: In this paper, a partial performance tradeoff modeling method is proposed for the hierarchical optimization of large analog systems. The key idea is to extract partial Pareto front model around the optimized block-level target performances instead of extracting the complete one. An iterative method based on Bayesian optimization is further proposed to update the partial model and, simultaneously, optimize the entire system. Our experimental results demonstrate that compared to the state-of-the-art methods, our proposed method can achieve a 3.0× cost reduction without surrendering any performances.

TECHNICAL SESSION

TS28. Mastering Synthesis Optimization

Chair: Yun Shao, Shenzhen Giga Design Automation Co., Ltd.

Time	16:00-18:10 | May 13, 2024	Venue	2-9 / Presidium Room

TAIK DETAILS

16:00-16:30 | Invited Talk | Lei Chen, Huawei Noah's Ark Lab, Hong Kong

Speech Title: Logic Synthesis Meets Artificial Intelligence

Invited Speaker's Bio: Lei Chen is a senior researcher at Huawei Noah's Ark Lab. His research interests include EDA logic synthesis, circuit data modeling, data-driven optimizations and big data management. He has been responsible for the research and development of various projects including logic synthesis. He has been dedicated to the research and development of key algorithms for logic synthesis. He has published more than 30 papers in top conferences and journals such as DAC, KDD, SIGMOD, ICDE, VLDB, TKDE. He has applied for over 10 patents.

Abstract: Electronic Design Automation (EDA) plays a fundamental role in modern circuit design, and logic synthesis is a crucial step in the EDA flow. With the advent of artificial intelligence (AI), various AI techniques have been applied to logic synthesis to enhance the efficiency and quality of circuit designs. This talk provides an overview of the state-of-the-art AI applications in EDA logic synthesis, covering machine learning, deep learning, reinforcement learning and large language models (LLMs), etc. We discuss the principles, methodologies, and use cases of each AI approach, along with their strengths, limitations, and recent advancements. Moreover, we will try to analyze the impact of AI/LLM for logic synthesis, exploring its potential to revolutionize traditional methods and enable the development of advanced and optimized circuits. We will also try to highlight challenges and suggestions for future research directions, emphasizing the promising prospects of AI/LLM for EDA logic synthesis.

16:30-16:50 | Paper ID: 167 | Zhang Hu, Ningbo University

Speech Title: A Novel Structural Choices Generation Method for Logic Restructuring

Author(s): Zhang Hu, Chengyu Ma, Zhufei Chu

Abstract: Logic restructuring is an efficient method for achieving conversions between different logic representations and optimizing logic network. However, as a mapping-based method, it often comes with structural bias issues. This will result in poor quality of logic restructuring. Therefore, we propose a novel structural choices generation method to address the issue of structural bias in logic restructuring. It matches the substructures of the network with the database of pre-computed optimum structures to obtain equivalent nodes. It can efficiently obtain many high-quality candidate structures and generate choice networks for different logic representations. The experimental results demonstrate that our method effectively improves the quality of results during logic transformation. In logic optimization, our approach achieves a 67.3% reduction in logic depth for test cases, with a 1.95% decrease in network size.

16:50-17:10 | Paper ID: 62 | Cunqing Lan, Fudan University

Speech Title: On Accelerating Domain-Specific MC-TS with Knowledge Retention and Efficient Parallelization for Logic Optimization

Author(s): Cunqing Lan, Xinyao Wang, Zijian Jiang, Hongyang Pan, Keren Zhu, Zhaori Bi, Changhao Yan, Xuan Zeng

Abstract: Recently, demand of higher quality of result (QoR) for logic optimization have spurred numerous studies on generating logic transformation sequence for specific objective. Nevertheless, previous works often

suffer from heavy reliance on computing resources or are stuck at local optima. In this work, We propose a logic transformation sequence generator based on a domain-specific Monte Carlo tree search (MC-TS). Our framework propose to utilizes information obtained from synthesis tools as context to guild the tree search. Additionally, we implement the algorithm with knowledge retention and adaptive parallelization for further acceleration. Experiments on open-source benchmarks of various scale show that our framework outperforms the state-of-the-art work, Alphasyn, with an average 20.11% efficiency improvement while maintaining comparable effectiveness.

17:10-17:30 | Paper ID: 46 | Chenyang Lv, Shanghai Jiao Tong University

Speech Title: ERL-LS: Accelerating Primitive Sequence Generation of Logic Synthesis with Evolutionary Reinforcement Learning

Author(s): Chenyang Lv, Boning Zhang, Weikang Qian, Zhezhi He

Abstract: In electronic design automation (EDA), logic synthesis (LS) converts a high-level description of a circuit to a gate-level netlist,generally using a unified heuristic algorithm to optimize different combinational circuits. Synthesized circuits often perform better, such as smaller areas and lower latency. Logic synthesis relies on a series of optimization commands to conduct the optimization, but the complexity of synthesis optimization flow increases exponentially with more commands used. Machine-learning-based methods, especially reinforcement learning (RL), are widely utilized in large-scale (LS) applications for efficiently exploring customized circuit design spaces. For rapid LS, we propose an Evolutionarily scheduled Reinforcement Learning(ERL) framework, which is compatible with various agents adopted in prior RL-based LS works. Owing to the parallel execution on a multi-core processor, it can significantly improve exploration efficiency without losing solution quality. Our experiments show that, on EPFL benchmark and executing with 4-cores, our framework with RL agent in DRiLLS generally achieves 3.37 times speed-up to reach global optimal compared to the corresponding work.

17:30-17:50 | Paper ID: 170 | Jun Zhu, Ningbo University

Speech Title: Multiplication Complexity Optimization Based on Quantified Boolean Formulas

Author(s): Jun Zhu, Hongyang Pan, Zhufei Chu

Abstract: In the field of cryptography and security, minimizing the number of AND gates within logic networks is crucial. Such optimization significantly influences the multiplication complexity of circuits. This paper proposes a Quantified Boolean Formulas (QBF) based resynthesis to dynamically construct local circuits from sub-circuits, with the goal of minimizing the number of AND gates and optimizing the number of XOR gate numbers in well-optimized networks. Experimental results on parts of the EPFL benchmarks suite indicate that the proposed method effectively reduces the number of AND gates by 15.51% and the number of XOR gates by 3.34%.

17:50-18:10 | Paper ID: 146 | Zhenghao Cui, Sun Yat-sen University

Speech Title: Automatic Multi-Parameter Tuning for Logic Synthesis with Reinforcement Learning

Author(s): Zhenghao Cui, Minghua Shen

Abstract: Logic synthesis serves as the intermediate stage between abstract logic and physical implementation. It involves various logic optimization and technology mapping algorithms,which are iteratively applied to the circuit. The multi-parameter tuning for logic synthesis is the process of generating a sequence of logic optimization and technology mapping operators with multiple parameters. The Quality-of-Result (QoR) is significantly impacted by different recursive arrangements of optimization commands and parameter selections of technology mapping operators. Nowadays, the order of calling algorithms is usually determined by heuristics. The heuristic becomes unacceptable if based on a large exploration space and test design. To address this issue, we utilize reinforcement learning (RL) with the proximal policy optimization (PPO) algorithm to train an agent to effectively generate the optimization and mapping sequence. To acquire adequate features to aid decision-making,we utilize the Graph Isomorphic Network (GIN) with edge feature aggregation capability to learn circuit representations and use circuit scalars as state representations for the reinforcement learning agent. To allow the agent to learn from historical operations, we utilize the Long Short-Term Memory (LSTM) to uncover the relationships between different operators within a single sequence. Additionally, we address the issue of

selecting the parameter for the technology mapping operator by framing it as a multi-class classification problem and training a classifier to identify the optimal parameter. We evaluated the effectiveness of our model using the EPFL arithmetic benchmark. The result shows that our model achieved an average improvement of 9.93%in area and 13.62% in depth on each test design over the greedy algorithm. Furthermore, we achieve a significant improvement of65.79% in area and 37.79% in delay on the biggest test design. These findings highlight the potential of our approach to enhance logic synthesis and technology mapping for large circuits.

TECHNICAL SESSION

TS29. Process Modeling and Simulation in Modern Era

Chair: Yijun Cui, Nanjing University of Aeronautics and Astronautics

Time	16:00-18:10 | May 13, 2024	Venue	3-3 / Hanzhong Hall

TAIK DETAILS

16:00-16:30 | Invited Talk | Geng Bai, GWX Technology

Speech Title: Empowering Next Generation IC Design and Manufacturing through Innovation

Invited Speaker's Bio: Geng Bai, CTO of Shenzhen GWX Technology Co., Ltd. He obtained bachelor's and master's degrees from the Department of Electronic Science at Nankai University in 1994 and 1996, respectively. In 2002, obtained a Ph.D. in Electrical Engineering from University of Illinois Urbana-Champaign. Dr. Bai Geng has 20 years of experience in developing EDA software tools and has worked at Synopsys and Nassda. He worked at Avatar (formerly known as Atoptech) from 2007 to 2019. During his tenure at Synopsys and Atoptech, Dr. Bai Geng personally developed a series of advanced algorithms and modules related to EDA. He holds four US patents related to EDA and has published more than six papers at major EDA conferences. At present, he is mainly responsible for the development of the full process EDA platform at Shenzhen GWX Technology. His research direction includes the development of EDA tools such as layout and wiring, verification, and physical verification in the design of ultra large scale integrated circuits.

Abstract: This report will focus on how the innovation of EDA tools can inject new vitality into the next-generation IC design and manufacturing, and explore how to improve data integrity and accelerate the design and manufacturing processes under the background of increasing globalization and complexity of IC manufacturing. Additionally, the report will analyze the process of using GPU technology to accelerate optical proximity correction (OPC) and the role of the modular architecture of general-purpose service engines in improving performance and efficiency. By combining embedded AI algorithms with GPU acceleration, unprecedented speed and accuracy can be achieved in computationally intensive tasks. Finally, the report introduces the concept of DTCO into the IC design and manufacturing stages, discussing how it can support manufacturing optimization for IC design.

The relevant research results have set new standards for performance, accuracy, and usability in the EDA industry, showcasing the application prospects of technological innovation in the face of challenges. We look forward to discussing the future development trends of EDA tools with industry peers, promoting innovation and cooperation, and jointly ushering in a new era of next-generation IC design and manufacturing.

16:30-16:50 | Paper ID: 125 | Rui Zhang, Semitronix Corporation

Speech Title: Adaptive Time-stepping Method for CMP Simulation Efficiency

Author(s): Rui Zhang, Yu-wei Xie, Qing Zhang, Huan Kan, Wei-wei Pan

Abstract: As process technology scales down and new materials are introduced, coupled with the escalating complexity of processes, enhancing yield in chip production becomes an increasingly formidable task. The incorporation of an important process, Chemical Mechanical Polishing (CMP), is designed to ensure the controlled surface morphology of each wafer, thereby augmenting chip production yield. Building upon the findings of T. Tugbawa et al., the parameterization of layout pattern feature extraction, in conjunction with the modeling of corresponding process steps in chip production, allows us to simulate and predict the entire process of surface morphology changes during CMP. This paper introduces the development of modeling and prediction software for CMP simulation processes (CMPEXP), grounded in the aforementioned research. An adaptive time

step iterative simulation strategy has been implemented in this study, resulting in an enhancement of simulation efficiency by approximately 150% compared to fixed time steps iteration.

16:50-17:10 | Paper ID: 201 | Yue Qian, University of Chinese Academy of Sciences

Speech Title: Utilizing Neural Networks for Automated Construction of Semi-Physical CMP Models

Author(s): Yue Qian, Lan Chen

Abstract: The planarization of chip surface after chemical mechanical planarization is more and more important which may cause DOF, IR drop, timing closure, EM problems. Given that CMP modeling encompasses the integration of multiple complex mechanisms, including physics, chemistry, and materials, enhancing the accuracy of traditional CMP models based solely on physical principles becomes challenging. The empirical relationships and con-stants in semi-physical models are typically manually specified by experts, resulting in minimal automation in model deployment. We propose utilizing neural networks to automate the construction of these relationships, thereby enhancing the automated construction of semi-physical CMP models. It incorporates well-established optimizers to speeds up training and significantly improves model accuracy. Experimental results indicate that our model competes with fully data-driven models, outperforms existing semi-physical models, and achieves a remarkable 30% reduction in RMSE with rapid training (fewer than 200 epochs).

17:10-17:30 | Paper ID: 203 | Zhirui Niu, University of Chinese Academy of Sciences

Speech Title: Performance Analysis of Different Processor Architectures Applied to CMP Process Modeling Acceleration

Author(s): Zhirui Niu, Yan Sun, Qin Du, Lan Chen

Abstract: The current research trend in microelectronics industry focuses on applying deep learning to Electronic Design Automation (EDA) to deal with the increasing computational demands. There is a rising requirement for higher computational power with the escalation of chip design scale and the complexity of chip performance analysis, thus the utilization of Data Computing Unit (DCU) or Graphics Processing Unit (GPU) with powerful parallel computing capabilities for acceleration becomes imperative. The Hygon Z100 DCU, a processor dedicated for large-scale data processing, has been extensively deployed in heterogeneous computing platforms. In this paper, a series of microbenchmark programs are designed based on the architecture of Hygon Z100 DCU and NVIDIA RTX 2080Ti GPU. Additionally, EDA softwares developed by the research group are ported to both computing platforms. The performance differences between the Hygon Z100 and NVIDIA RTX 2080Ti are tested, and their acceleration capabilities in EDA applications are compared. Due to the higher number of stream processors and additional tensor cores dedicated for accelerating matrix operations in the RTX 2080Ti GPU, it demonstrates higher acceleration performance compared with the Hygon Z100 in EDA applications.

17:30-17:50 | Paper ID: 88 | Xinchang Wang, Guangdong Greater Bay Area Institute of Integrated Circuit and System

Speech Title: Application of a CFD Simulation on Spin Coating Process

Author(s): Xinchang Wang, YunWang, Yansong Liu, Yajuan Su, Yayi Wei, Tianchun Ye

Abstract: In this study, a three-dimensional spin coating model has been built up to simulation the flow formation process of Lagrange droplets in photoresist coating process. Numerical calculation was performed by using the commercial computational fluid dynamics (CFD) package with a Reynolds-averaged Navier-Stokes (RANS) equation solver and a realizable k-ε two-layer model. The effects of the spin speed, dispensed volume, solvent saturated vapor pressure, initial photoresist viscosity on the film thickness and uniformity have been examined with different spin coating process parameters and material parameters. The initial photoresist viscosity and saturation vapor pressure are important parameters that affect the average film thickness. The spin-coating process of a wetting recipe was simulated using the model and compared with an recipe without wetting. The wetting recipe involves spraying 2.5cc of PGMEA solvent during static conditions, followed by the addition of 1cc of Lagrange photoresist droplets within 4.8 seconds. In contrast, the recipe without wetting injects 2cc of droplets at low speed. At the completion of the entire recipe, the wetting recipe exhibits an improved average film thickness compared to the typical recipe, it shows that wetting recipe can realized the purpose of photoresist reduction.

17:50-18:10 | Paper ID: 171 | Hong Chen, GWX Technology

Speech Title: Line Edge Roughness Modeling for Continuous Time-space Resist Simulations

Author(s): Hong Chen, Li Xie, Lijie Wei, Zhong Shu, Binglin Qiu, Zhuoran Pei, Geng Bai

Abstract: Resist line edge roughness (LER) is generally regarded as noise inherent in every lithography processing step. Current state of art LER simulators model the physical causes of LER rigorously at each step, including the variation in optical source, resist material and PEB/development processes, and by using a set of stochastic, multi-scale numerical algorithms. With a high level of complexity involved, computational cost is often unacceptable for practical usage on larger patterning areas. Another disadvantage of the current LER models requires a significant modification for the existing simulation flow and numerical solvers, incurs a high R&D overhead and difficulties in industrial adoption. This work proposed a semi-empirical but straightforward LER simulation method that works around all the difficulties in current LER modeling. By introducing an appropriate amount of randomness to the system using LER parameters, it is possible to produce the desired LER in a resist simulation. LER is therefore a natural result in a numerical simulation due to the randomness carried by the initial value.

TECHNICAL SESSION

TS30. Compact Modeling for Circuit Innovation

Chair: Fangfang Zhao, Primarius Technologies

Time	16:00-18:00 | May 13, 2024	Venue	3-6 / Yulin Hall

TAIK DETAILS

16:00-16:20 | Paper ID: 26 | Siyuan Zhang, Huazhong University of Science and Technology

Speech Title: A Verilog-A Compact Model for Four-Wave Mixing Supporting Electronic-Photonic Co-Simulation

Author(s): Siyuan Zhang, Xiaolong Fan, Nuo Chen, Ken Xingze Wang, Jing Xu, Min Tan

Abstract: A Verilog-A compact model for four-wave mixing (FWM) is proposed in this brief. It is fully compatible with existing EDA platforms, and can support the rapid electronic-photonic co-simulation. The model avoids the description of the complicated physical process of the FWM, and provides an easy way for system designers to monitor the changes of the key optical parameters, thus accelerating the co-design and co-optimization of the hybrid systems containing FWM process. The framework and the key derivations for modeling are presented, and the simulation results of our model agrees well with numerical full-map results.

16:20-16:40 | Paper ID: 76 | Xiang Su, University of Electronic Science and Technology of China

Speech Title: Recent Progress of AlGaN/GaN HEMTs QPZD Model

Author(s): Xiang Su, Shuman Mao, Yuehang Xu

Abstract: This paper summarizes the recent advances in compact modeling techniques based on the Quasi-Physical Zone Division (QPZD) theory mainly for AlGaN/GaN HEMTs. Firstly, the modeling principle of QPZD and the corresponding core model is introduced. A comprehensive comparison between the QPZD model and other well-known compact models is also presented. For high-power design applications, the modeling techniques of dispersion effects including self-heating effects, ambient temperature effects, and trapping effects are well developed. Furthermore, several efforts have been devoted to the extension of QPZD model capability. Details of the microwave noise model, switch model, and process fluctuation model are introduced, respectively. Owing to these efforts, the developed QPZD modeling techniques can contribute to the comprehensive and accurate designs of significant chips in RF front-ends.

16:40-17:00 | Paper ID: 82 | Hong Cai Chen, Southeast University

Speech Title: Modeling and Circuit Implementation of Complex Nonlinear Component Behavior Based on Attention-Assisted BiLSTM

Author(s): Zeng Hui Chang, Hong Cai Chen

Abstract: Recent advancements in neural network-based behavioral modeling approaches have profoundly influenced the modeling and simulation of radio frequency (RF) devices and circuit modules. This manuscript elucidates the constraints inherent in the existing body of literature with regard to accurately encapsulating the intricacies of nonlinear components. It introduces an innovative modeling paradigm designed to surmount these challenges. Moreover, the incorporation of neural ordinary differential equations into the modeling framework permits a more adaptable simulation step input, thereby augmenting the modeling process. The efficacy of the proposed model is validated through its application to PIN diodes within high-power microwave environments. Parameters of the model are meticulously extracted, and the inference mechanism is seamlessly integrated into circuit modules utilizing the VerilogA language. This integration substantially elevates the practical applicability of the model in circuit simulations.

17:00-17:20 | Paper ID: 122 | Wenbin Wang, Xidian University

Speech Title: Improving the Continuity and Smoothness of the Compact Model for Organic Light-Emitting Diode

Author(s): Wenbin Wang, Cong Li, Haokun Li, Xiaoming Li, Shaoxi Wang, Hailong You

Abstract: A compact model for organic light emitting diodes (OLED) is reported, which include current-voltage characteristics and capacitance-voltage characteristics for all regions. Compared with the previously published model, it not only expands the scope of application of the model, but also makes the model have better continuity and smoothness while ensuring accuracy. The model is continuous in the whole region through smooth functions and parameters, which provides convenience for circuit simulation. After parameter extraction, the model is in good agreement with the experimental measured data.

17:20-17:40 | Paper ID: 135 | Xiaobao Zhu, Peking University

Speech Title: Impacts of Parasitic Effects on PCM-based Neuromorphic Circuits under Advanced Technology Nodes

Author(s): Xiaobao Zhu, Baokang Peng, Feilong Ding, Ziyu Xie, Yihan Chen, Lining Zhang

Abstract: The limit of Parasitic Effects in terms of number of synapses is estimated for phase-change-memory based neuromorphic circuit under scaling technology nodes following ITRS. Parasitic capacitance components are evaluated for a 55nm process and extrapolated to other nodes. A memory compact model is used to study the effects of the capacitance on firing and weight updating in synapses, which provides design constraint for posterior bitline load estimation. The estimated maximum number of synapses indicate decreasing bitline load capacity due to intensified impact of parasitic capacitance along scaling feature size. The proposed estimation methodology is applicable to advanced nodes to provide quick evaluation for neuromorphic circuit design.

17:40-18:00 | Paper ID: 187 | Xinyue Zhang, Peking University

Speech Title: Modeling the Temperature-dependence of Silicon Diode with Fermi-Dirac Statistics down to 50K

Author(s): Xinyue Zhang, Fangxing Zhang, Cong Shen, Zirui Wang, Runsheng Wang, Lining Zhang, Ru Huang

Abstract: In this work, we present a comprehensive study of silicon diode current characteristics from room to cryogenic temperatures by experimental measurement, TCAD simulation, and physics model down. For the first time in the diode current model, we employ the Fermi-Dirac statistic to calculate the Fermi levels for solving the carrier degeneration problem at low temperatures, while considering the incomplete ionization on the series resistance effect. The temperature dependence of built-in potential, and the forward and reverse current of the silicon diode are analyzed and modeled. Our model prediction has good agreement with calibrated TCAD in the temperature range from 50K to 300K. This work advances the temperature-dependence diode models, while effectively evaluating the parasitic PN junction currents in CMOS technology at cryogenic temperature.

POSTER SESSION

Time	15:30-16:00 | May 11, 2024	Venue	Foyer of Theater Hall

PAPER DETAILS

Poster No.: Poster 01
Paper ID: 9
Paper Title: Contour Extraction Assists in Distinguishing Lithographic Hotspot
Author(s): Liuye Meng, Kun Ren, Dawei Gao, Yongyu Wu
Presenter: Liuye Meng, Zhejiang University

Poster No.: Poster 02
Paper ID: 15
Paper Title: Parallel DGTD Algorithm with LTS Scheme for Electrical Large Problems Based on Supercomputer
Author(s): Wenhao Liu, Liang Chen, Ping Li
Presenter: Wenhao Liu, Shanghai Jiao Tong University

Poster No.: Poster 03
Paper ID: 16
Paper Title: Learning Peak Temperature in 3DICs by Deep Differentiable Forest
Author(s): Yingshi Chen, Min Zhu, Xueyin Zhang, Chunyang Feng
Presenter: Chenyang Lv, Shenzhen Giga Design Automation Co., Ltd.

Poster No.: Poster 04
Paper ID: 24
Paper Title: Pattern Match in VLSI Layout with Window Dance
Author(s): Zhiping Mou, Kun Ren, Dawei Gao, Shibin Xu
Presenter: Zhiping Mou, Zhejiang University

Poster No.: Poster 05
Paper ID: 25
Paper Title: A GPU-Accelerated Harmonic Balance Method for Nonlinear Radio-Frequency Circuit Simulation
Author(s): Zhengzhuo Wang, Yanliang Sha, Lingyun Ouyang, Quan Chen, Jianguo Hu, Deming Wang
Presenter: Zhengzhuo Wang, Sun Yat-sen University

Poster No.: Poster 06
Paper ID: 37
Paper Title: A High-precision De-embedding Method for GaAs IPD Wafer-level Testing
Author(s): Lingmei Ma, Xiaotian Song, Christine Tan, Wei Yao, Rong Qian, Liang Wu
Presenter: Lingmei Ma, Shanghai Institute of Microsystems and Information Technology, Chinese Academy of Sciences

Poster No.: Poster 07
Paper ID: 60
Paper Title: Research on Thermal Resistance Matrix of Multi-chip Module Based on Aluminum Nitride Ceramic Substrate
Author(s): Zhanqi Zhu, Junqin Zhang, Renhao Song, Guangbao Shan
Presenter: Zhanqi Zhu, Xidian University

Poster No.: Poster 08
Paper ID: 86
Paper Title: A Relative-Priority Encoding Genetic Algorithm for Integrated Mapping and Scheduling Optimization
Author(s): Zhifang Sun, Shengjie Jin, Jinxue Duan, Junqiang Jiang, Zebo Peng
Presenter: Zhifang Sun, Hunan Institute of Science and Technology

Poster No.: Poster 09
Paper ID: 94
Paper Title: CDE: A Novel CGRA Development Environment with Fast Design Space Exploration Framework
Author(s): Sichao Chen, Yuan Dai, Jide Zhang, Huizhen Kuang, Xuchen Gao, Wai-Shing Luk, Wenbo Yin, Lingli Wang
Presenter: Sichao Chen, Fudan University

Poster No.: Poster 10
Paper ID: 95
Paper Title: Automatic Adder Tree Re-Synthesis Tool for Digital Compute-in-Memory Low-power Optimization
Author(s): Wencong Wu, Shasha Guo, Hongyi Zhang, Xuxia Zhong, Chengchen Wang, Haozhe Zhu, Haidong Tian, Xiaoyang Zeng, Chixiao Chen
Presenter: Wencong Wu, Fudan University

Poster No.: Poster 11
Paper ID: 100
Paper Title: An Innovative and Efficient Unified Analysis Model for AlGaN/GaN HEMTs
Author(s): Baoqin Zhang, Junjie Feng, Yujie Han, Chuanzhong Xu, Fei Yu, Shuting Cai
Presenter: Baoqin Zhang, Huaqiao University

Poster No.: Poster 12
Paper ID: 119
Paper Title: Framework Independent Modeling for SRAM-Based In-Memory Computing
Author(s): Sicun Li, Ning Zhang, Wenbo Zhang, Runhua Yang, Yuchun Chang, Botao Xiong
Presenter: Ning Zhang, Dalian University of Technology

Poster No.: Poster 13
Paper ID: 174
Paper Title: Co-optimization of Circuit Aging and Thermal Resilience: Buffer Insertion and Gate Sizing
Author(s): Ling Xiong, Wangyong Chen, Mingyue Zheng, Linlin Cai
Presenter: Ling Xiong, Sun Yat-sen University

Poster No.: Poster 14
Paper ID: 176
Paper Title: Neural Network-based Classification of Breakdown Mechanisms and Prediction of Breakdown Voltage and On-resistance for 4H-SiC Trench Gate MOS Devices
Author(s): Jiaxi Zhang, Shiyan Zhang, Ze Sun, Yucheng Wang, Yupan Wu, Wei Li, Shaoxi Wang
Presenter: Jiaxi Zhang, Northwestern Polytechnical University

Poster No.: Poster 15
Paper ID: 181
Paper Title: Single Event Upset and Radiation Hardening of the Complementary FET (CFET) based 6T-SRAM
Author(s): Zhengxin Zhang, Wangyong Chen, Jianwen Lin, Linlin Cai
Presenter: Zhengxin Zhang, Sun Yat-sen University

Poster No.: Poster 16
Paper ID: 204
Paper Title: The Hypergraph Partitioning Benchmark Suite
Author(s): Fang Zhang, Liyan Yu, Shunyang Bi, Pengfei Chu, Jing Tang, Hailong You
Presenter: Fang Zhang, Xidian University

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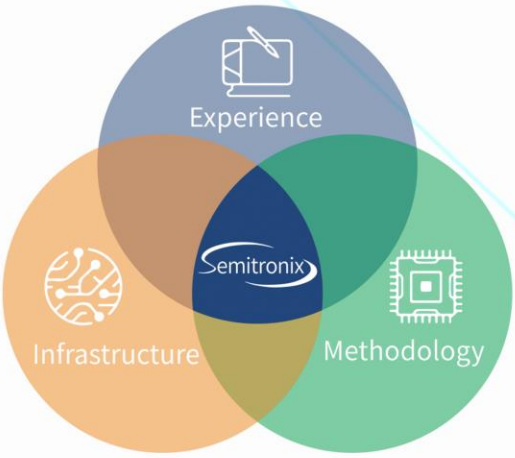

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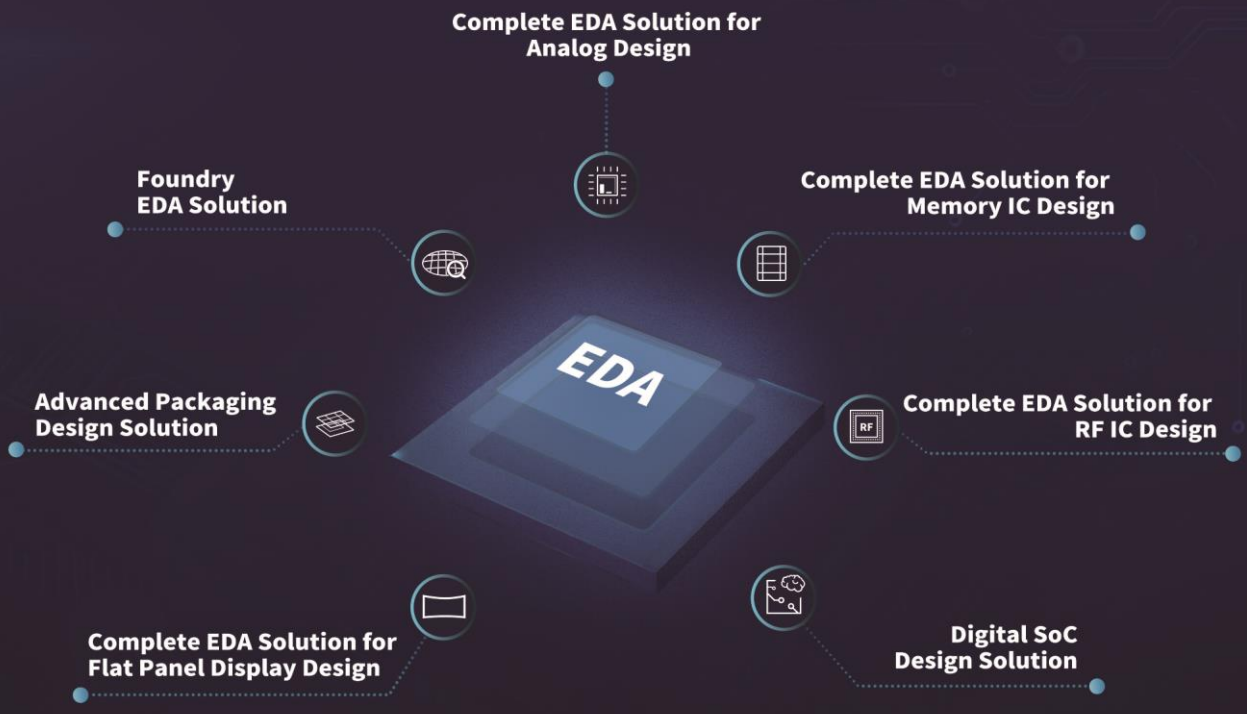

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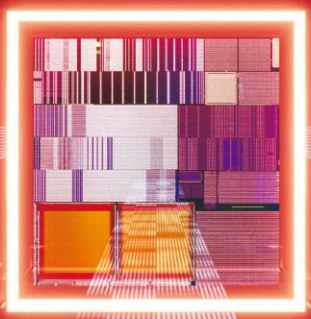

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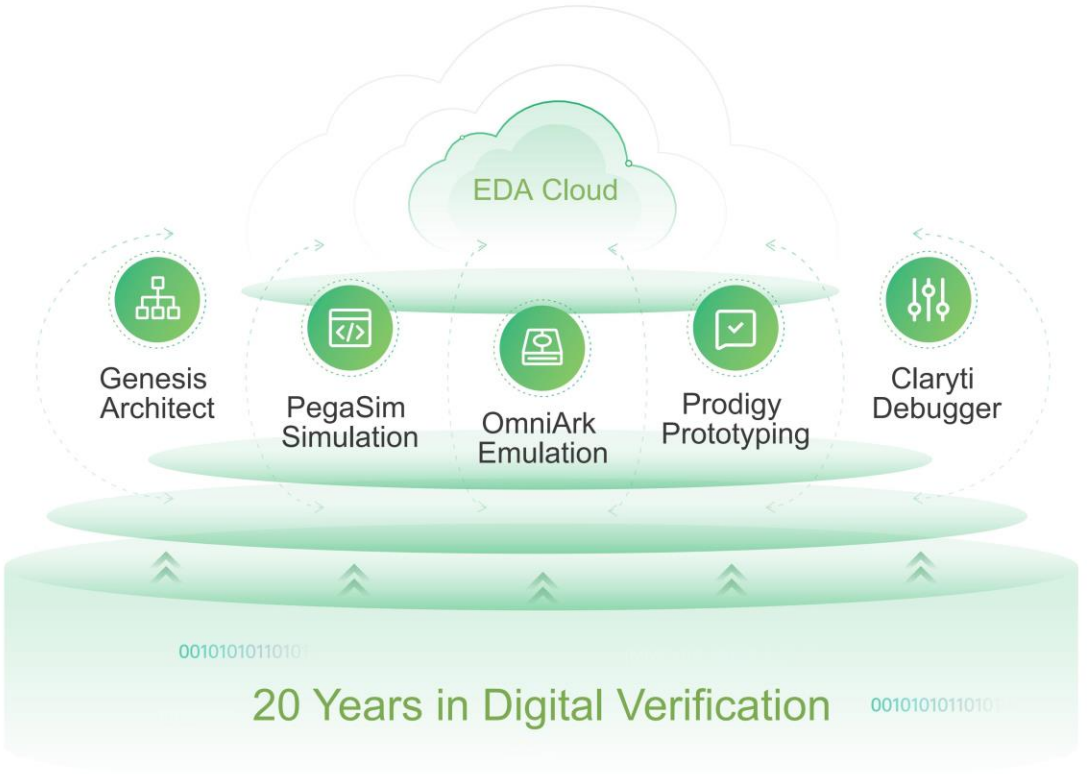

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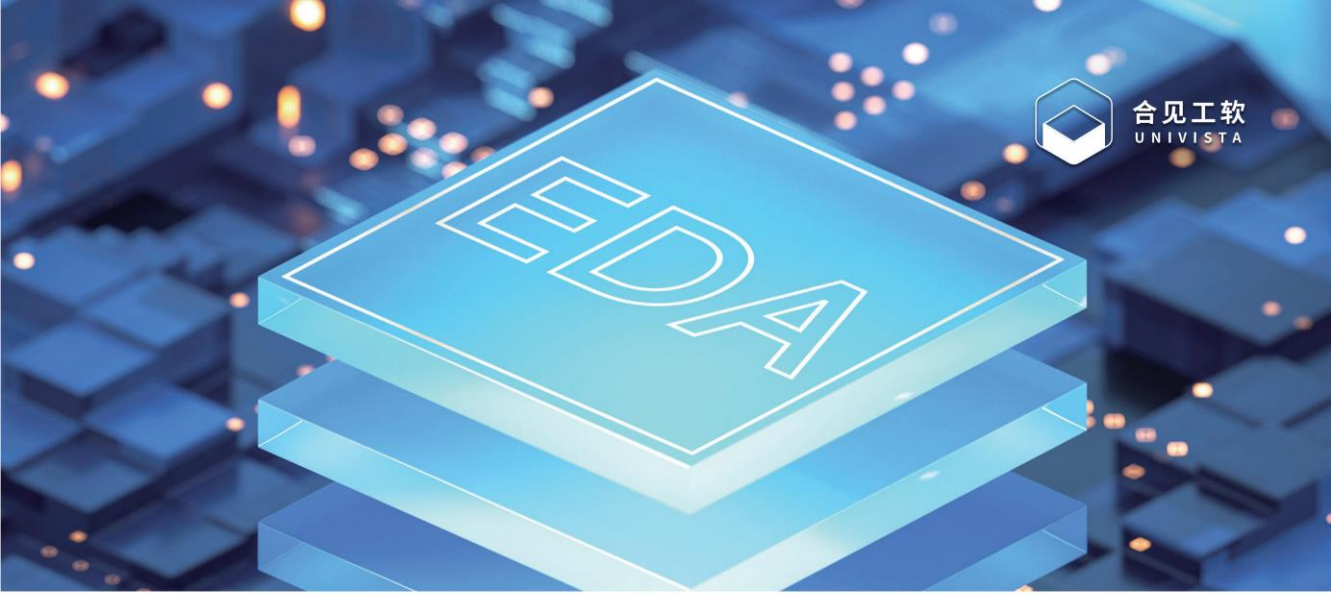

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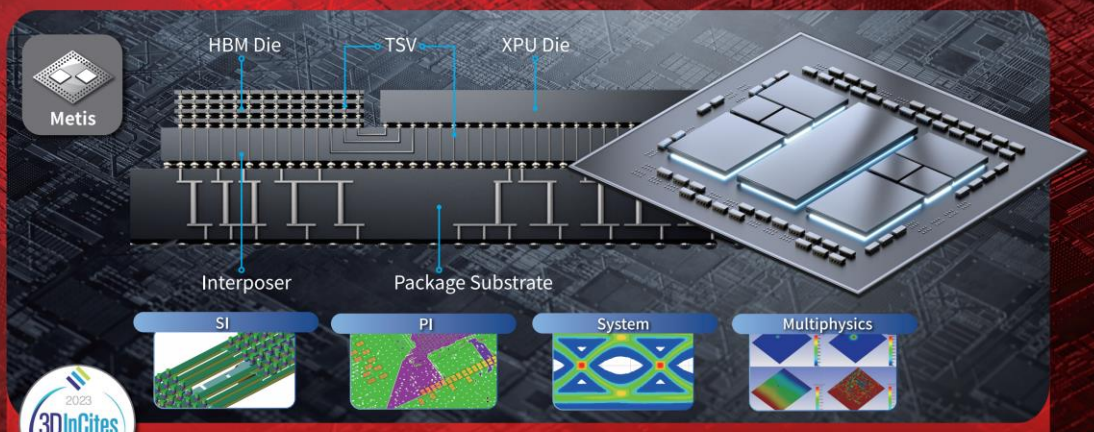

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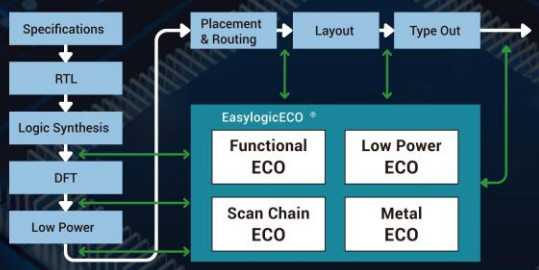

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EnnoCAD Electronics Technology Co., Ltd. is a cutting-edge EDA company that provides innovative EDA tools and solutions. The EnFortius® low-power EDA tools can effectively assist IC design engineers in analyzing and optimizing low-power design-related issues. The EnAltius® static verification tools can enhance code quality early in the design flow. The EnCitius® System Verification Studio is a full-stack cloud-based solution for SoC and system-related verification. In addition, EnnoCAD offers complete and customizable front to back design services for block and SoC level designs.

DONGFANG JINGYUAN ELECTRON LIMITED

PROVIDER OF YIELD MANAGEMENT SOLUTIONS IN INTEGRATED CIRCUIT FIELD

Dongfang Jingyuan Electron Co., Ltd. was established in 2014, headquartered in Beijing Yizhuang Economic and Technological Development Zone. The company focuses on integrated circuit production management. Since its establishment, the company has been insisting on innovation research and development 191 domestic and foreign invention patents, 67 authorized invention patents and 15 software copyrights have been declared. And 26 registered trademarks. As a talent of high-tech enterprises is fundamental. 70% of the total number of R&D personnel, of which 8% are doctorates and 53% are masters.Core members have product development and management experience in the world's top semiconductor technology companies located in Silicon Valley, Japan and Europe.

- Founded in **2014**
- Participate in the **National** IC-related Projects
- **Top-Tier** Products Leading Domestically Competitive Globally
- Employees **550+**
- Orders Fully Booked with Positive Customer Feedback
- Proactive Yield Enhancement Solutions

PRODUCT MATRIX

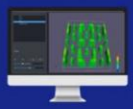
EBI
ELECTRON BEAM DEFECT INSPECTION

CD-SEM
CRITICAL DIMENSION-SCANNING ELECTRON MICROSCOPE

DR-SEM
DEFECT REVIEW-SCANNING ELECTRON MICROSCOPE

PanGen
PANGEN OPC

PanSim
SEMICONDUCTOR LITHOGRAPHY SIMULATOR



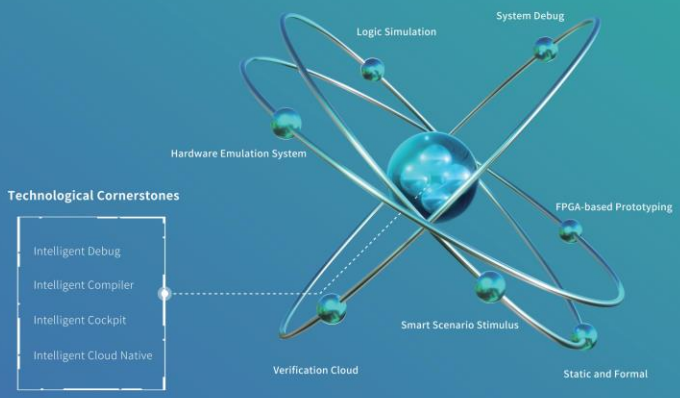
YieldBook
YIELD MANAGEMENT SYSTEM

Web: www.dfjy-jx.com Tel: +86-10-80823200 Add: Building 12,156#,4th Jinghai Rd,BDA,Bejing 100176 P.R.China.

X-EPIC

Accelerating System Verification

Together with our partners, we are pursuing to bring the EDA industry to an entirely new level by injecting the power of Artificial Intelligence, Machine Learning, Cloud Native, and other leading-edge technologies, which can enormously simplify and lower down the bar of the current IC design. In the end, it shortens the development cycle or time-to-market of the product.



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Shanghai LEDA Technology

LEDA Introduction

LEDA Technology is a provider of EDA solutions, currently focusing on physical implementation for digital ICs. Our physical implementation solution, LeCompiler, is based on the fused RTL-to-GDSII and DTCO concepts, emphasizing multi-step co-optimization between/among logic synthesis, placement, routing and sign-off.
LEDA is continuing to evolve LeCompiler, developing it into an end-to-end physical implementation solution to meet demanding PPA requirements of cutting-edge designs and help customers realize their innovative design ideas.

LeCompiler Introduction

Based on a unified data model, LeCompiler employs a set of innovative algorithms to optimize timing, power and congestion. With ML-based advanced optimizations, LeCompiler can globally place and route large modern designs while meeting user-provided physical and timing constraints and advanced process technology constraints.
The solution has been verified in a variety of high-performance customer designs, showing very competitive results. Some of the LeCompiler capabilities such as automated floorplanning and physical optimization have been integrated into customers' design flows and are in production use.

Shanghai / Fuzhou / Beijing / Changsha info@ledatech.cn

MEMO

MEMO

ADVISORS

IEEE/CEDA, ACM/SIGDA

Department of Information Science, National Natural Science Foundation of China (NSFC)

Chinese Institute of Electronics (CIE)

Steering Committee, Major Plan of "Fundamental Research on Post-Moore Novel Devices"

ORGANIZERS

EDA Ecosystem Development Accelerator (EDA²)

EDA Committee of CIE

SUPPORTERS

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